A Vertical C_{60} Transistor with a Permeable Base Electrode

DISSERTATION

zur Erlangung des akademischen Grades

Doctor rerum naturalium
(Dr. rer. nat.)

vorgelegt

der Fakultät Mathematik und Naturwissenschaften
der Technischen Universität Dresden

von

Dipl. Phys. Axel Fischer

geboren am 29.04.1986 in Oschatz

Eingereicht am 18.12.2014
Verteidigt am 11.09.2015

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Die Dissertation wurde in der Zeit von 11/2010 bis
12/2014 im Institut für Angewandte Photophysik angefertigt.

TECHNISCHE
UNIVERSITÄT
DRESDEN

TU Dresden Fakultät Mathematik und Naturwissenschaften, Institut für Angewandte Photophysik

Dissertation

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Submitted on 18. December 2014
Defended on 11. September 2015

ABSTRACT

English

A high performance vertical organic transistor based on the organic semiconductor C_{60} is developed in this work. The sandwich geometry of this transistor, well known from organic light-emitting diodes or organic solar cells, allows for a short transfer length of charge carriers in vertical direction. In comparison to conventional organic field-effect transistors with lateral current flow, much smaller channel lengths are reached, even if low resolution and low-cost shadow masks are used. As a result, the transistor operates at low voltages (1 V), drives current densities in the range of 10 A/cm^2, and enables a switching speed in the MHz range. The operation mechanism is studied in detail. It is demonstrated that the transistor can be described by a nano-porous permeable base electrode insulated by a thin native aluminum oxide film on its surface. Thus, the transistor has to be understood as two metal-oxide-semiconductor diodes, sharing a common electrode, the base. Upon applying a bias to the base, charges accumulate in front of the oxide, similar to the channel formation in a field-effect transistor. Due to the increased conductivity in this region, charges are efficiently transported toward and through the pinholes of the base electrode, realizing a high charge carrier transmission. Thus, even a low concentration of openings in the base electrode is sufficient to ensure large transmission currents.

The device concept turns out to be ideal for applications where high transconductance and high operation frequency are needed, e.g. in analog amplifier circuits. The full potential of the transistor is obtained if the active area is structured by an insulating layer in order to perfectly align the three electrodes. Besides that, molecular doping near the charge injecting contact is essential to minimize the contact resistance.

Due to the high power density in the vertical C_{60} transistor, Joule self-heating occurs, which is discussed in this work in the context of organic semiconductors. The large activation energies of the electrical conductivity observed cause the presence of S-shaped current-voltage characteristics and result in thermal switching as well as negative differential resistances, as demonstrated for several two-terminal devices. A detailed understanding of these processes is important to determine restrictions and proceed with further optimizations.

Deutsch

In dieser Arbeit wird ein vertikaler organischer Transistor mit hoher Leistungsfähigkeit vorgestellt, der auf dem organischen Halbleiter C_{60} basiert. Die von organischen Leuchtdioden und organischen Solarzellen bekannte 'Sandwich'-Geometrie wird verwendet, so dass es möglich ist, für die vertikale Stromrichtung kurze Transferlängen der Ladungsträger zu erreichen. Im Vergleich zum konventionellen organischen Feldeffekttransistor mit lateralem Stromfluss werden dadurch viel kleinere Kanallängen erreicht, selbst wenn preisgünstige Schattenmasken mit geringer Auflösung für die thermische Verdampfung im Vakuum genutzt werden. Daher kann der Transistor bei einer Betriebsspannung von 1 V Stromdichten im Bereich von 10 A/cm^2 und Schaltgeschwindigkeiten im MHz-Bereich erreichen. Obwohl diese Technologie vielversprechend ist, fehlt bislang ein umfassendes Verständnis des Funktionsmechanismus. Hier wird gezeigt, dass der Transistor eine nanoporöse Basiselektrode hat, die durch ein natives Oxid auf ihrer Oberfläche elektrisch isoliert ist. Daher kann das Bauelement als zwei Metall-Oxid-Halbleiter-Dioden verstanden werden, die sich eine gemeinsame Elektrode, die Basis, teilen. Unter Spannung akkumulieren Ladungsträger vor dem Oxid, ähnlich zur Ausbildung eines Ladungsträgerkanals im Feldeffekttransistor. Aufgrund der erhöhten Leitfähigkeit in dieser Region werden Ladungsträger effizient zu und durch die Öffnungen der Basis transportiert, was zu hohen Ladungsträgertransmissionen führt. Selbst bei einer geringen Konzentration von Löchern in der Basiselektrode werden so hohe Transmissionsströme erzielt.

Das Bauelementkonzept ist ideal für Anwendungen, in denen eine hohe Transkonduktanz und eine hohe Schaltgeschwindigkeit erreicht werden soll, z.B. in analogen Schaltkreisen, die kleine Signale verarbeiten. Das volle Potential des Transistors offenbart sich jedoch, wenn die aktive Fläche durch eine Isolatorschicht strukturiert wird, um den Überlapp der drei Elektroden zu optimieren, so dass Leckströme minimiert werden. Daneben ist die Dotierung der Molekülschichten am Emitter essentiell, um Kontaktwiderstände zu vermeiden.

Aufgrund der hohen Leistungsdichten in den vertikalen C_{60}-Transistoren kommt es zur Selbsterwärmung, die in dieser Arbeit im Kontext organischen Halbleiter diskutiert wird. Die große Aktivierungsenergie der Leitfähigkeit führt zu S-förmigen Strom-Spannungs-Kennlinien und hat thermisches Umschalten sowie negative differentielle Widerstände zur Folge, was für verschiedene Bauelemente demonstriert wird. Ein detailliertes Verständnis dieser Prozesse ist wichtig, um Beschränkungen für Anwendungen zu erkennen und um entsprechende Verbesserungen einzuführen.

CONTENTS

PUBLICATIONS, PATENTS AND CONFERENCE CONTRIBUTIONS

Publications

- Axel Fischer, Philipp Siebeneicher, Hans Kleemann, Karl Leo, and Björn Lüssem, "Bidirectional operation of vertical organic triodes", Journal of Applied Physics, **2012**, vol. 111, p. 044507
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Patents

- US 2013/0277651 A1 "Vertical Organic Transistor and Production Method"
- US 2014/0284567 A1 "Vertical Organic Transistor, Circuit Configuration and Arrangement with Vertical Organic Transistors and Method of Manufacturing"
- Nicht, Fischer et al. filed in **2013** Topic: Functionalized p-dopants as self-assembled monolayers

Conference contributions

- Axel Fischer, René Michel, Philipp Sebastian, Hans Kleemann, Alexander Zakhidov, Björn Lüssem, and Karl Leo; Plastic Electronics **2010**, Dresden; "Vertical Organic Triodes" - Poster
- Axel Fischer, Philipp Sebastian, Hans Kleemann, Alexander Zakhidov, Björn Lüssem, and Karl Leo; DPG **2011**, Dresden; "Vertical Organic n-Triodes based on Me-PTCDI and fullerenes" - Poster
- Axel Fischer, Philipp Sebastian, Hans Kleemann, Björn Lüssem, and Karl Leo; ICOE **2011**, Rome; "Bidirectional working mechanism in Vertical Organic n-Triodes" - Poster
- Axel Fischer, Paul Pahner, Björn Lüssem, Karl Leo, Reinhard Scholz, Thomas Koprucki, Jürgen Fuhrmann, Annegret Glitzky, and Klaus Gärtner; DPG **2012**, Berlin; "Positive feedback between Joule heating and current density in organic devices based on C_{60}" - Talk

- Axel Fischer, Paul Pahner, Björn Lüssem, Karl Leo, Reinhard Scholz, Thomas Koprucki, Jürgen Fuhrmann, Klaus Gärtner, and Annegret Glitzky; ICOE **2012**, Tarragona; "Self-heating in vertical n-doped / intrinsic / n-doped C_{60} devices" - Talk
- Axel Fischer, Reinhard Scholz, Karl Leo, and Björn Lüssem; MRS **2013**, San Francisco; "A High Current C_{60} Vertical Organic Transistor Comprising Doped Injection Layer" - Poster
- Axel Fischer, Reinhard Scholz, Karl Leo, and Björn Lüssem; DPG **2014**, "Dresden; OLED - a light emitting thermistor?" - Talk
- Axel Fischer, Thomas Koprucki, Annegret Glitzky, Matthias Liero, Klaus Gärtner, Daniel Kasemann, Björn Lüssem, Karl Leo, and Reinhard Scholz; SimOEP **2014**, Mallorca; "Negative differential resistance in OLEDs due to nonlinear electrothermal feedback modelled by a 2D thermistor network" - Talk

1 INTRODUCTION

Our daily life is increasingly influenced by technological advances. Nowadays, being without computer or connection to the world wide web is hardly imaginable for many people. Mobile phones have greatly changed the way we are connected to people all around the world. Information is exchanged between various devices, consisting of e.g. keyboards or loudspeakers, or simply by touching and viewing displays. Furthermore, important data, documents, and pictures are nowadays stored on electronic media like hard disks, memory sticks, or directly in the cloud. Thus, the way we interact and communicate is strongly related to achievements in electronics and more specifically in semiconductor technologies. Each of these devices is based on transistors, tiny integrated components which are able to amplify electronic signals, and which are able to switch their conductance over orders of magnitude, allowing them to process logic signals in larger assemblies. A modern personal computer processor has more than one billion transistors integrated into a single chip. For comparison, a book typically contains less than a million characters. Therefore, the semiconductor transistor has revolutionized the world and initiated the information age.

Even before the first realization of a transistor[1] by Bardeen and Brattain in 1947 [1], devices with a similar function existed: For example, a relay controls the current by mechanically shortening two wires using the electromagnetic field of a coil. One of the first analytic engines, the Zuse Z3, was based on relays, which are relatively heavy and slow. Later on, vacuum tube triodes have been increasingly used for that purpose, as realized by de Forrest already in 1907 [2]. Such electron tubes are fully operational amplifiers, consisting of three electrodes, the cathode, the anode, and a grid, placed in a high vacuum. As they are based on purely electric effects, they reach much higher switching speed than relays, but they are large and typically require high voltages in the range of 100 V to drive them.

The advantages of semiconductor transistors are apparent: They can be miniaturized, operated at low voltages, and reach high switching speeds. Furthermore, advanced structuring technologies like photolithography allow for the integration of multiple devices into a single circuit. This

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[1] At that time called a semiconductor triode, deduced from the greek "tri hodos" (three ways) related to the number of terminals.

is achieved by using inorganic semiconductor materials, such as Si, Ge, or GaAs. Intrinsically, they are non-conductive but their crystal structure enables the incorporation of impurity atoms, like boron or phosphorus, releasing holes (p-type) or electrons (n-type), respectively. By this doping process, the conductivity of the semiconductor can be intentionally adjusted. Sophisticated functionality appears if the type of conduction changes in the crystal, forming a pn-junction on which devices like light-emitting diodes (LED) or solar cells are based on. Adding a third layer, i.e. realizing npn or pnp stacks, a bipolar junction transistor (BJT) evolves. Each of the regions is contacted to an electrode called emitter, base, and collector. If the base thickness is very thin, i.e. in the range of microns, majority charge carriers injected at the emitter are able to cross the base by diffusion and reach the collector. To control this current flow, a much smaller base current consisting of minority charge carriers is necessary, so that current amplification is obtained [3].

However, the breakthrough of computer technology is related to the realization of metal-oxide-semiconductor field-effect transistors (MOSFETs) in 1960. These transistors are based on Si as the semiconductor and SiO_2 as the insulator [4]. The idea has been first proposed by Lilienfeld around 1930 [5]. An insulated gate contact allows for controlling the conductivity of a semiconductor between a source and a drain contact by a field effect. Thus, the current flowing through the device is varied by orders of magnitude. In contrast to the bipolar transistor, no gate current is necessary for device operation, making the unipolar charge flow in the transistor fully controlled by voltage, ideal for applications where logic states, e.g. on and off, have to be processed. Nowadays, MOSFETs are highly optimized using a very thin gate insulating layer of a few nanometers, whereas the so called channel length between the source and drain contact is of the order of a few 10 nm. As a consequence, very high switching speeds in the GHz range are achieved [6].

Besides these conventional approaches using inorganic semiconductors, the field of organic electronics started in the late 80’s. At that time, it was shown that organic devices can either emit light or convert light into electric current [7, 8]. To reach light emission, thin molecular layers have been placed between planar electrodes, resulting in a ’sandwich’-geometry and the perpendicularly arranged electrodes form a crossbar structure. In comparison to inorganic electronics, charge carrier mobilities of molecular layers are much lower, so that the performance in terms of current densities and switching speed cannot compete with conventional technologies. However, there are many other advantages: Molecules can be processed at low temperatures, avoiding high energy consumption and cost-intensive fabrication. This also allows for fabrication on flexible substrates made of plastic, because all steps are carried out below 150 °C. Furthermore, organic materials can be processed by different procedures. For example, they can be evaporated in vacuum, spin-coated, or simply printed from vapor or solution. The thickness of deposited layers can easily be controlled in the nanometer range while large areas can be covered with material. Thus, new applications can be thought of, such as bendable or even stretchable electronics. A further advantage is the versatility of organic materials. Some of them are transparent, enabling transparent electronics, e.g. used for displays. Furthermore, organic molecules exist which strongly absorb light in the visible range, allowing for realization of very thin solar cells. Hence, the most important application of organic electronics, the organic light-emitting diode (OLED) and the organic solar cell (OSC), offer a wide range of new possibilities. Both devices benefit from the fact that a high charge carrier mobility as obtained for Si is not needed, and upscaling to large areas with high uniformity can be done due to the sandwich geometry combined with a minimum of material usage. Furthermore, crossbar electrodes enable a simple and inexpensive structuring of the devices.

In 1987, the first organic field-effect transistor was presented [9]. Its structure resembles the MOSFET with the difference that molecular layers are used as the semiconducting materials, and no doped regions exist. As the transistor can be processed layer by layer on individual substrates and does not depend on a wafer as substrate, the device is also named organic thin film transistor (OTFT). Nowadays, the performance of such OTFTs outperforms similar devices using amorphous Si, the standard material for TFTs used in flat panel displays. The typical advantage of OLEDs and OSCs to be processable on large areas is not important for these transistors anymore. Indeed, the deposited material can cover a large area and thus be used for a large number of devices at the same time. However, structuring of the electrodes with feature sizes in the lower µm range limits the capability of the technique. Generally, one can assume that the smaller the feature size, the better the performance of a transistor becomes in terms of current and switching speed. In contrast to inorganic materials, structuring by photolithography is limited by materials compatibility issues in organics and is still under investigation. Thus, electrodes are typically fabricated on organic semiconductors by evaporation through a metal shadow mask. For large feature sizes (several 10 µm), such masks can be inexpensively processed by laser cutting, whereas masks with small feature sizes in the range of microns can become very expensive. To establish a low-cost technology for production of organic transistors, it is worthwhile to use the experience of producing OLEDs with the advantages of the 'sandwich'-geometry combined with the crossbar electrode design in order to fabricate organic transistors. This technological approach is referred to as vertical organic transistors. Three planar electrodes separated by functional layers are brought to an overlap in the desired active area, where one of the electrodes is able to control the current flow between the other two. One of these concepts is the vertical organic triode which is the topic of this work.

A vertical organic triode consists of three planar metal electrodes, separated by organic semiconductor layers (cf. Fig. 1.1). The middle electrode is very thin, allowing charge carriers to be transmitted from one organic layer to the other, but it still forms a conductive electrode to which an electric potential can be applied. A current injected at the top electrode (emitter) can then flow through the middle electrode (base) and finally is collected by the lower electrode (collector). Only a small percentage of the emitter current drops into the base, resulting in a current amplification, defined as the ratio of collector and base current. The electrodes are structured by evaporation through cheap and low resolution shadow masks with feature sizes of 100 µm. However, the vertical channel length defined by the layer thicknesses is in the range of 100 nm, and thus much smaller compared to conventional lateral OFETs. Depending on the organic material, unipolar VOTs of n-type or p-type can be fabricated, conducting either electrons or holes, respectively.

The idea of a vertical organic triode has been introduced 20 years ago by Yang and Heeger, who developed an organic device with a polymer grid base electrode [10]. However, the first device showing low operation voltage together with high current densities and a pronounced current amplification was published by Fujimoto *et al.* in 2005 [11]. Despite the progress made in this field, a comprehensive understanding of the operation mechanism has not been reached. Especially, the transmission process of charge carriers through the base electrode remained unclear. There are essentially two concepts borrowed from inorganic semiconductors. The first is a metal-base

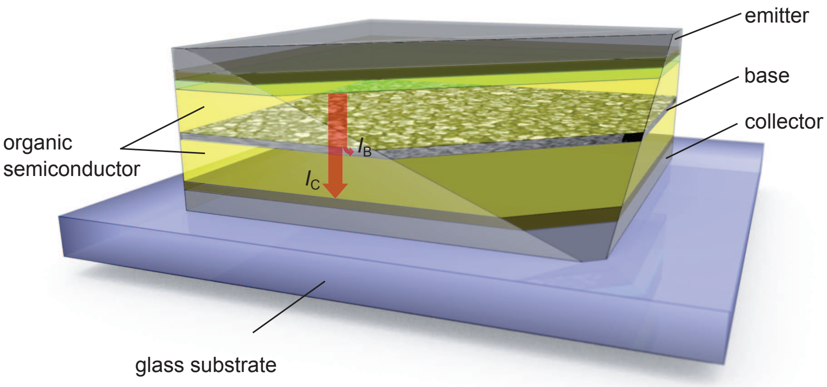

Figure 1.1: A 3D sketch of a vertical organic triode. The current is injected at the top electrode (emitter), is mainly transmitted through the middle electrode (base), and finally conducted to the bottom electrode (collector). Only a small percentage of the injected current drops into the base, so that a current amplification originates. The green layer underneath the top electrode indicates that this device concept allows for inserting easily further functional layer, e.g. to improve charge injection.

transistor which has a closed base electrode of uniform thickness, thin enough to allow charge carriers to be transmitted by incomplete relaxation of hot carriers. In this context, also tunneling through the base electrode is discussed, which can be enforced by thin insulating films surrounding the base electrode. Another concept is a permeable base transistor, consisting of a regular structured base electrode with defined openings, typically in the range of the thickness of the device. It is still a matter of debate which of the above concepts applies for vertical organic triodes or if there even exists a further one. If the device works like a metal-base transistor, the question arises why the transmission factor can reach exceptionally high values of more than 99% in experiment, although the inorganic equivalent hardly reached 50%. Furthermore, high transmission can be observed for both operation directions, using the top or the bottom electrode as the emitter, in sharp contrast to theoretical predictions relying on the metal-base transistor. In case of a permeable base transistor, the question arises how to explain the high transmission in the absence of intentionally structured openings in the base electrode. However, this feature is the highlight of a vertical organic triode: One can demonstrate a transistor operation although the metal film acting as the base is homogeneously deposited, making the device structuring easy in comparison to other transistor technologies. Even if small pinholes form in the metallic layer which act as a direct connection between the upper and the lower semiconductor, one has to ask why charges should flow through tiny openings, sufficiently small to remain hidden in standard characterization methods. Instead, it seems to be more plausible that charges flow into the base.

The situation becomes even more complex because several devices are published in literature using different materials for the upper semiconductor layer, the lower semiconductor layer, and the base electrode, so that it remains unclear whether all these devices rely on the same operation mechanism. Therefore, it is the intention of this work to figure out a reliable material system to build a vertical organic triode, allowing for a detailed analysis of the device characteristics. Special attention is given to a symmetric design with respect to the base electrode. For example, the upper and the lower semiconductor material consist of the same material, so that differences in the molecular energy levels do not play a role. In the past years, the performance of vertical organic triodes has been improved, but one can show that the recent performance does not exceed conventional lateral OFETs. By introducing the molecule C_{60} as the basic material for all semiconductor layers and by using a highly efficient doped layer for improved charge injection, it will be shown that a vertical organic triode is a serious candidate to overcome present limitations of conventional organic transistor concepts. Advantages include very high current densities and switching speed, enabling operation in the MHz range at a minimum effort for structuring the device. Hence, this work aims at demonstrating the competitiveness of vertical organic triodes with respect to other technologies by understanding their current prospects and limitations.

This work is structured in three introductory chapters and five chapters presenting the results. At the beginning, a theoretical section summarizes basic principles of organic semiconductors. It is explained how molecules mainly consisting of carbon form and assemble into a larger arrangement allowing to conduct charges if an external electric field is applied. Based on this knowledge, recent organic transistor technologies are introduced and compared with a special focus on OFETs, being the standard device, and the VOT, being the device discussed in this work. An experimental chapter gives an overview about techniques that have been used in order to fabricate and characterize the samples investigated. The results start with a chapter explaining basic device characteristics of a standardized sample, serving as the platform for further studies and optimization steps. A second and a third result chapter describe investigations about the working mechanism of the device, demonstrating that annealing as well as oxidation of the base electrode are essential fabrication steps for producing VOTs with high performance. Based on these studies, the understanding of the device operation is significantly enhanced, allowing for an optimization of the overall performance. Important improvements of the device are reached by insertion of a functional layer enhancing the charge injection and by device structuring enabling a reliable downscaling of the lateral dimensions as presented in a fourth result chapter. A last chapter discusses the aspect of self-heating under the point of view of laterally extended and planar organic semiconductor devices, improving the understanding of the thermistor problem.

2 THEORY

Semiconductivity of molecular films is introduced in this chapter, based on the properties of aromatic organic molecules. It will be shown how hybridization of carbon atoms leads to stable molecules with partially delocalized electrons which is essential to understand the interaction between molecules in an organic solid. The resulting rearrangement of the energy levels eventually causes the characteristic distribution of states. The delocalization of electrons on the molecule is further important for efficient charge transfer between adjacent molecules. Current models describing the charge transport in organic semiconductors are presented.

A second section addresses the physics of semiconductor devices. The basics are summarized, allowing for the calculation of the field and charge carrier distribution as well as the current flow in a semiconductor layer. Besides charge transport, understanding injection of charge carriers into the semiconductor is of importance. Therefore, the contact formation at interfaces between metals and organic semiconductors is discussed which directly influences the contact resistance. In order to reach the highest possible currents in vertical organic triodes, both, charge transport and injection, have to be optimal. After that, the characteristics of Schottky diodes and metal-oxide-semiconductor (MOS) capacitors are presented which are both related to MOS diodes, a basic component of the vertical organic triode as shown later on. MOS diodes include an oxide layer, thin enough to allow for charge transport by tunneling. As a last point, electrothermal feedback in semiconductor devices showing Joule self-heating is presented under the aspect of a thermally activated sample conductivity.

2.1 FROM SMALL MOLECULES TO CONDUCTING THIN FILMS

2.1.1 Aromatic hydrocarbons

Organic materials are carbon compounds with some exceptions, e.g. carbon allotropes or CO_2. These substances occur in gaseous, liquid, or solid phase under ambient conditions, and they

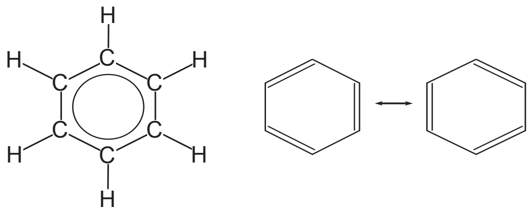

Figure 2.1: Structural formula of benzene C_6H_6 (left). The molecule consists of a carbon ring with conjugated double bonds and one hydrogen atom bound to each carbon atom. For clarity, structural formulas as shown on the right omit the hydrogen. Two equal configurations of the conjugation are the reason for electrons of the π orbitals to be delocalized, indicated by a ring in the left structural formula.

form the basis for life on earth. One can distinguish between small molecules and macromolecules. The former have a size in the range of 1 nm and a weight of several 100 u, the latter can be much larger and heavier.[1] For organic electronics, small molecules and polymers are relevant because they are able to conduct charges, making them interesting for electronic applications. In contrast to small molecules, polymers are macromolecules with a periodic repetition of molecular subunits (monomer). In that way, molecular chains of varying length can be created by concatenating monomers. Polymers are well known as the base material for plastics. Both kinds of compounds can be used to fabricate organic LEDs, organic solar cells, or organic transistors [12]. Small molecules and polymers further differ in the way they are processed, in their chemical stability, and their electronic properties. In this work, the focus is on small molecules which indeed rely on a more complex processing in vacuum but offer superior performance in terms of charge transport.

The number of organic molecules is quite large and not all of them show electrical conductivity. Most relevant are aromatic hydrocarbons being widely employed in organic electronics. They consist of carbon rings having conjugated double bonds. The simplest representative is the molecule benzene C_6H_6, shown in Fig. 2.1a). However, being a liquid under ambient conditions, it is not used as an organic semiconductor. The molecule consists of a single ring of six carbon atoms having a sixfold rotational symmetry. At each corner, a hydrogen atom attaches to a free bond of the ring structure. The C-C distance is ca. 140 pm and oppositely lying hydrogen atoms have a distance of about 500 pm [13]. Between neighboring carbon atoms single and double bonds alternate. Due to the symmetry of the molecule, there are two equal configurations having the same energy, and the solution for the probability function has to be built by a linear combination of both. Electrons which are part of a double bond are able to relocate by changing the conjugation configuration. As a consequence, a delocalized electron system originates on the molecule. This behavior can be adopted to larger molecules, consisting of several carbon rings attached to each other by joining their carbon ring edges. In such planar molecules, a network of conjugated double bonds allows electrons to be delocalized over the whole carbon ring system.

This conjugation is caused by a hybridization of the carbon atom orbitals, namely sp^2 hybridization. Carbon has the electron configuration $1s^2 2s^2 2p^2$. Thus, the two electrons of the L shell with p orbitals, orthogonal to each other, can bind with other atoms. The corresponding rectangular molecules of carbon atoms are highly unstable [14]. However, by a linear combination of the

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[1] 1 atomic mass unit (1 u) equals ca. 1.661×10^{-27} kg, defined as one twelfth of the mass a neutral ^{12}C atom has.

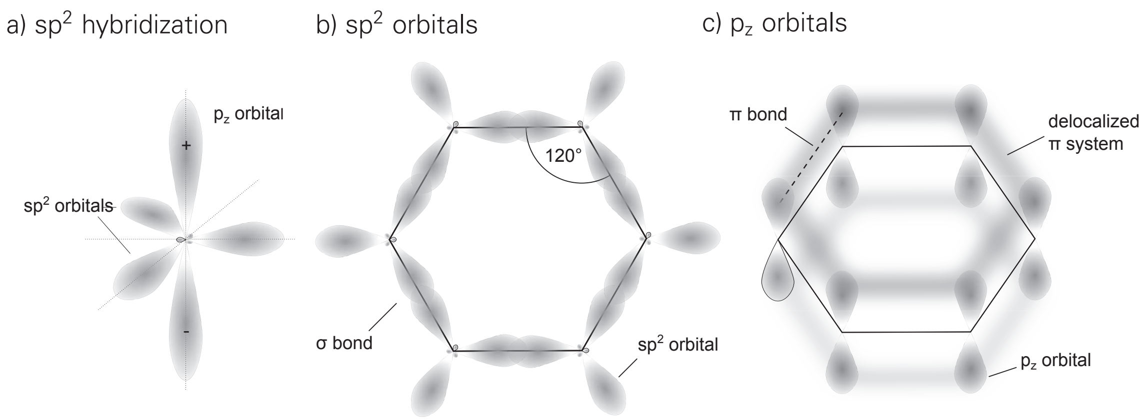

Figure 2.2: Orbitals and bonds in a carbon ring. a) A single sp^2-hybridized carbon atom. b) Topview onto the sp^2-hybridized orbitals in a carbon ring configuration. Their overlap leads to strong σ-bindings. c) Isometric view onto the p$_z$ orbitals, symmetrically extending above and below the atom plane. A delocalized π system forms by π bonds of the atomic p$_z$ orbitals.

atomic orbitals, hybridized orbitals are obtained, realizing more stable bonds with other hybridized carbon atoms of the same type. Depending on the number of participating p orbitals, sp, sp^2, or sp^3 hybridization states are formed. For example, sp hybridization leads to a linear arrangement of the atoms with a bond angle of 180°. This is the case for acetylene C_2H_2 where the two carbon atoms have a triple bond and two hydrogen atoms are attached. In the case of ethylene C_2H_4, a sp^2 hybridization takes place with a trigonal arrangement of the orbitals and a bond angle of 120°. This type of binding is also found in the carbon allotropes graphite and graphene, resulting in the typical honeycomb structure. If an s electron promotes to a p orbital, carbon is further able to show sp^3 hybridization. The tetrahedral configuration of the hybridized orbitals (bond angle: 109.5°) is present in ethane C_2H_6, having a single bond between the carbon atoms but six hydrogen atoms attached. A sp^3 hybridization is further found in diamond where it results in a face-centered cubic crystal structure with a tetrahedral arrangement of the bonds around each carbon atom. The previous examples demonstrate that the different types of hybridization have a large impact on the chemical bonds between carbon atoms and consequently determine the molecular or solid structure and with that the properties of the resulting material.

For planar hydrocarbons, sp^2 hybridization is most important. Two of the three available 2p orbitals hybridize together with the 2s orbital to three sp^2 orbitals filled each by one electron, and one p$_z$ orbital remains. Figure 2.2a) shows the resulting orbitals of a carbon atom, neglecting the 1s orbital. The sp^2 orbitals span a plane on which the p$_z$ orbital aligns perpendicularly. Due to the threefold rotational symmetry of the orbitals, carbon rings of 6 atoms form whose optimally overlapping sp^2 orbitals realize σ bonds. This can be seen in Fig. 2.2b). The residual sp^2 orbital of each carbon atom protrudes from the ring and can either be bond to a further carbon atom, building larger networks of carbon rings, or to hydrogen, as in the case of benzene discussed above. Further, the free bond can be used to attach other atoms or side chains which can be utilized to tune the energy levels and the electron distribution of the molecule. In Fig. 2.2c), the interaction of the p$_z$ orbitals is visualized. Neighboring orbitals can form π bonds which are weaker than the σ bond due to the lower overlap of the wavefunctions. Since every carbon atom has two adjacent atoms but only one electron in the p$_z$ orbital, double bonds of π and σ bonds arise in conjugated form. As discussed above, the delocalized π system results then from two superposition of equal configurations of alternating π bonds.

The transition from a single carbon atom to an aromatic molecule involves the transition from atomic orbitals to molecular orbitals. Figure 2.3 shows the energy diagram of benzene. On the left, the energy levels of a single carbon atom are given in the ground state and after hybridization. Whereas electrons in atomic orbitals are located close to the atom, molecular π orbitals are extended over the whole molecule, able to represent the delocalization of the electrons. In order to construct the molecular orbitals, again a linear combination of the atomic orbitals is done. The molecular orbitals should represent the symmetry of the benzene molecule, so that the molecular wave functions are chosen as symmetric or antisymmetric combinations of the atomic orbitals with respect to the central symmetry point of the molecule [13]. For example, the region of the p_z orbital where the wavefunction has e.g. positive values (cf. Fig. 2.2a)) can be above or underneath the molecule plane. As depicted in the right of Fig. 2.3, for the six atomic p_z orbitals, six independent combinations can be found, each representing a molecular orbital. Generally, the number of atomic orbitals and molecular orbitals remains the same. The resulting molecular orbitals have a bonding (π) or an antibonding (π^*) character, depending on the presence of nodes between the atoms. In such a node plane, the probability of presence reaches zero as a consequence of inversely oriented p_z orbitals on neighboring atoms. Then, these atoms rather repel each other and favor a geometric expansion of the molecule. If the probability of electron presence between two atoms does not reach zero, an effective attraction occurs. The lower the number of node planes, the lower the energy of the state is. The splitting of the energy levels is approximately symmetric to the original energy levels as derived by the Hückel method, so that three molecular orbitals with a higher (antibonding) and three with a lower energy (bonding) are formed [13]. The shift in energy directly correlates with the overlap of the atomic orbitals by the transfer integral

$$J_{ij} = \int \phi_i^*(\vec{r}) V(\vec{r}) \phi_j(\vec{r}) d^3 r \tag{2.1}$$

where ϕ_i,ϕ_j denotes the wavefunctions of the orbitals of two different atoms i, j and $V(\vec{r})$ is the potential [13]. Filling these states with electrons of antiparallel spin, all bonding molecular orbitals are filled and all antibonding molecular orbitals are unfilled. As a consequence, the benzene molecule is stable and energetically favored with respect to six single carbon atoms. Similarly, molecular orbitals arise from the sigma bonds, again forming six bonding (σ) and six antibonding (σ^*) linear combinations of the atomic orbitals. However, due to the larger overlap of the sp^2 orbitals, the energy split between bonding and antibonding molecular orbitals is more pronounced here. Their energies clearly fall below or exceed the energies of the π molecular orbitals, respectively. Besides that, further molecular orbitals originate from the interaction with the hydrogen atoms in the case of benzene which are not shown in Fig. 2.3 and will be not discussed here.

This behavior applies not only to benzene but can be extended to other aromatic molecules. It remains similar that all bonding π orbitals are completely filled in the ground state of the molecule whereas the antibonding states are unfilled. One can understand this as a first prerequisite for an organic molecule to show semiconducting behavior because an energy gap is automatically formed between the highest occupied molecular orbital (HOMO) and the lowest unoccupied

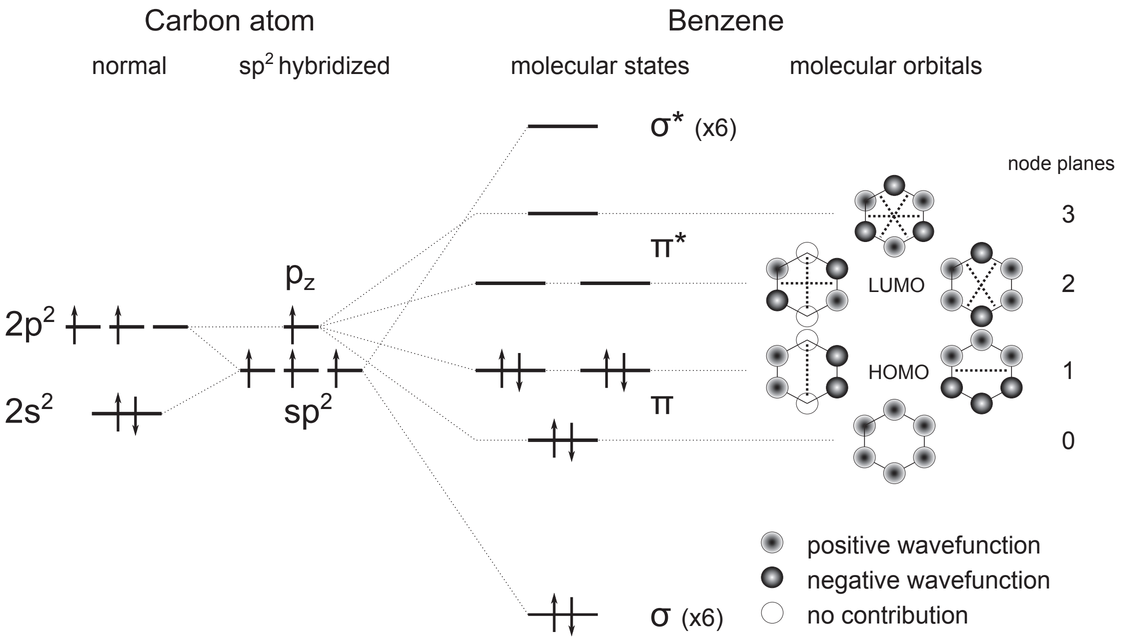

Figure 2.3: Left: A carbon atom in ground state configuration and after sp^2 hybridization. Right: Energy levels of the benzene molecule and graphical representation of the molecular orbitals with their node planes. For simplicity, energy levels corresponding to bonds with hydrogen atoms are not shown.

molecular orbital (LUMO). The energy gap

$$E_\mathrm{g} = E_\mathrm{LUMO} - E_\mathrm{HOMO} \tag{2.2}$$

is given by the energetic distance of the LUMO and the HOMO level. In order to change these energy levels, one can slightly modify the molecules. By following certain design rules, it is possible to 'tune' the molecular characteristic which will in turn affect the properties of the corresponding organic semiconductor. For example, increasing the spatial size of the delocalized π system results in a reduction of the energy gap E_g [15, 16]. This can be seen in molecules with different numbers of carbon rings attached in a row. From benzene C_6H_6 (1 ring) to pentacene $C_{22}H_{14}$ (5 rings), the energy gap in the gaseous phase decreases symmetrically to the mid gap position from more than 10 eV to close to 5 eV. In another design strategy, the peripheral hydrogen atoms are replaced by side groups, shifting the HOMO and LUMO level position of the molecular derivatives upwards or downwards, or introducing a polarity to the molecule. Further modifications can change the shape and structure of the molecule in order to influence the arrangement in organic solids, or they make the molecule more stable under ambient conditions. There are several other relations between the structure of the organic molecule and the macroscopic properties resulting from that. Here, it can be concluded that the strength of organic molecules lies in their large variability realized by the methods and the construction tools of organic chemistry. Thus, compounds can be synthesized which are optimized for specialized purposes.

2.1.2 Solid state physics of molecular materials

Not every molecule is a solid at ambient conditions which is an inevitable prerequisite in order to use them as organic semiconductors. Generally, atoms or molecules stick together if attractive and repulsive forces exist which neutralize each other in a stable equilibrium position. Repulsive components can be explained by the Coulomb interaction between the positive atom cores as well as between electrons. Furthermore, the Pauli principle has to be fulfilled, stating that fermions have to differ in at least one quantum number if they share the same position. Thus, electrons cannot stay in regions where similarly occupied orbitals of two molecules overlap [16]. Then, the corresponding potential is often described by $\propto r^{-12}$, leading to an adequate description of experimental results [17, p. 503].

Stable aromatic molecules are not able to make covalent bonds to other molecules, similar to the C-C or C-H bonds in the benzene molecule, since all electrons are already incorporated in bonding orbitals. Thus, this strong type of bond is excluded between organic molecules. If further covalent bonds are possible larger molecules would automatically form until no more electrons are available for additional covalent bonds. In case of two molecular species, there might be an ionic binding or a charge transfer complex between the different molecules, resulting in a crystal lattice where both molecules occur with an equal number within the unit cell [16]. However, these models cannot be used to explain the binding of molecules of the same type because they would be equally charged or a reason is missing justifying a permanent charge transfer between them.

Most aromatic molecules are indeed neutral and nonpolar, but dipoles can easily be induced by a displacement of the delocalized π-electron system. Therefore, van-der-Waals forces, describing the interaction between induced dipoles, are used to explain the attraction of molecules. In case of molecules with no permanent dipole moment, instantaneously induced dipoles on a molecule polarize the surrounding molecules, leading to opposite dipoles and an attraction. Then, both dipoles stabilize each other, and these so called London dispersion forces describe the attraction between two molecules with a corresponding potential $\propto -\alpha_\mathrm{p}^2 r^{-6}$ [16]. The polarizability of the molecule α_p is defined by the dipole strength p_ind an external electric field F can induce on the molecule.

Both components, repulsive and attractive, are added to obtain the effective potential, describing the binding between the molecules. The following form with the molecule specific coefficients A and B

$$V(r) = A\frac{1}{r^{12}} - B\frac{1}{r^6} \tag{2.3}$$

is called Lennard-Jones potential, schematically shown in Fig. 2.4. It can be seen that a global energetic minimum exists, determining the equilibrium state. There might be other shapes of the repulsive potentials leading to a similar result, but important for a stable bond is that the repulsive term decays much faster than the attractive term with increase of molecular distance r. Then, the length r_eq relates to the distance between two bound molecules whereas the dissociation energy ϵ_eq can be associated with the binding energy, defined with respect to fully separated molecules at $r \to \infty$ having zero energy. A typical binding strength of aromatic molecules is in the range of several 10 meV and thus similar to the thermal energy $k_\mathrm{B} T_0 \sim 25\,\mathrm{meV}$ at room temperature T_0,

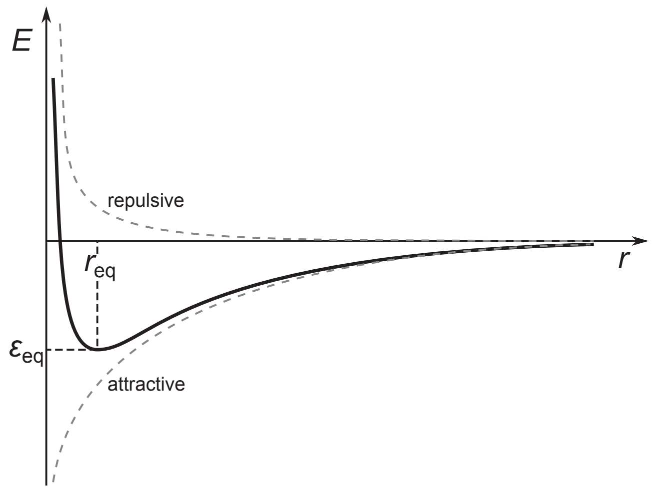

Figure 2.4: Lennard-Jones potential, consisting of an attractive and a repulsive part. The energy minimum determines the distance r_{eq} at which two molecules are in a stable equilibrium position and their binding energy is ϵ_{eq}.

with k_{B} as the Boltzmann constant. The thermal energy can be seen as a mean energy a system can receive or release in thermal equilibrium. For a stable and permanent bond between two molecules as needed for a solid, $\epsilon_{\text{eq}} > k_{\text{B}}T_0$ should be fulfilled. Otherwise, thermally induced energy fluctuations would already be able to detach two molecules from each other, resulting in a liquid or gaseous phase of the material. In that sense, London dispersion forces have a strength which does not necessarily lead to an organic solid at ambient temperatures. The binding energy determines the melting point of the material to be below (liquid, gaseous) or above (solid) the ambient temperature. As shown above, the attractive potential is proportional to the square of the polarizability. Thus, molecules with a larger delocalized π-system typically involve larger binding energies, because the dipole moment increases if the distance between the separated charges increases. For example, comparing benzene with one carbon ring to tetracene having four carbon rings in a row, one finds an increase of the melting point from 5.5 °C to 357 °C [16].

Organic solids can have different morphology, being crystalline or amorphous. Crystalline structures form if molecules favor a certain arrangement to each other. This can be e.g. motivated by their shape and the orientation of the molecular orbitals. A special case are planar aromatic hydrocarbons such as anthracene or pentacene. The electrons of the π-electron system are mainly located above and underneath the molecular plane. Thus, the electron cloud of each molecule can come very close to the neighbors one, so that a strong interaction arises. Generally, crystals are described by a unit cell, typically containing one or two molecules, which repeats quasi-endlessly in all directions [16]. A general triclinic unit cell is determined by their lattice constants a,b, and c being the length of the edges, and the three lattice angles α, β, and γ, defined by the positioning of the unit cell's boundary planes. Planar organic molecules often crystallize in a herringbone structure, having a monoclinic ($\alpha = \beta = 90° \neq \gamma$) or triclinic lattice crystal system. The unit cell consists of two molecules which are tilted to each other along their longitudinal axis (cf. Ref. [18]). Typical lattice constants are in the range of 5 Å to 10 Å. Another type of crystallization is given by direct π-π stacking [19]. The molecule planes are now parallel to each other and the molecules stack over each other. Depending on the structure of the delocalized π system, molecules can be aligned in sandwich form, joining a common symmetry axis, or parallel but displaced [20]. In all cases, molecules of the crystal are invariant by translations of the lattice vector. This further implies that they find exactly the same environment in different lattice cells upon this operation. In contrast to that, amorphous organic solids are formed if a preferred arrangement does not exist between the molecules or several equal arrangements exist which alternate irregularly. Then, a periodicity is not observed, and the solid cannot completely be characterized by a few parameters as in the case of a crystal. However, one can use distribution functions, e.g. to characterize the spatial disorder. Assuming a Gaussian distribution of molecular distances, the distribution of the distances between nearest neighbor molecules can be given by

$$G(\Gamma) = \frac{1}{\sqrt{\pi\Sigma}} \exp\left[-\frac{(\Gamma-\Gamma_0)^2}{\Sigma}\right] \tag{2.4}$$

where Σ characterizes the spatial disorder and $\Gamma - \Gamma_0$ is the difference to the mean distance, defined as unitless numbers by $\Gamma_0 = \gamma a$. Here, a is the mean intermolecular distance, and γ is the inverse localization radius which results from the electronic coupling between the molecular orbitals [21, 22]. As discussed later, spatial disorder has to be considered to correctly describe the transition probability of charges between neighboring molecules. Usually, amorphous materials are either weakly bound and have a low melting point, or they tend to recrystallize at higher temperatures, e.g. obtained for Spiro compounds [23].

The degree of crystallization strongly depends on the processing conditions. For example, even molecules with a stable crystalline lattice tend to show a polycrystalline phase if they are evaporated to achieve thin films. These molecules are not able to form a single crystal, because all over the substrate crystals start to grow with uncorrelated orientation. Many single crystals grow and build grains which meet and form grain boundaries where the periodicity of the crystal is disturbed. The growth can be influenced by the substrate temperature, the rate of the material flow, or the substrate material by changing the sticking of the first molecular monolayer [24, 25]. Whereas single grains of polycrystalline layers can be as thick as the layer thickness of vertical organic devices ($\sim$100 nm), organic materials with nanocrystalline morphology have a crystallite size in the range of 10 nm. This is the case if molecules, impinging on the substrate, orient less on the substrate or the last molecular layer, so that repeatedly new grains form. Evaporated thin films consist then of clusters of various large crystallites and the crystallinity does not extend over the typical thickness of a vertical organic device. The transition to amorphous organic solids is often blurred because nanocrystalline material might be partially amorphous. At the same time, polycrystalline materials might also have nanocrystalline character, indicating that these materials show a distribution of crystallite sizes. Other processing techniques, like recrystallization from solution or using a single crystal as the nucleus for further crystal growth have demonstrated that organic single crystals can be formed even on larger scale (up to several cm) [16, 26].

2.1.3 Energetic landscape of an organic semiconductor

Energy states of the molecule The HOMO and the LUMO level of each molecule play a key role in understanding organic semiconductors. Other states, e.g. levels lying lower the HOMO or above the LUMO are always occupied or unoccupied, respectively. Because the concentration of free charge carriers in the semiconductor cannot exceed the number of molecules per unit volume due to prohibitively high Coulomb interaction, the LUMO and HOMO states are sufficient to accomodate them. Thus, further discussions can be restricted to these two levels. Figure 2.5 shows the evolution from the states of a neutral molecule in the gas phase to the states obtained in an organic solid for an ionized molecule. A single neutral molecule has a HOMO and a LUMO defined by an ionization energy I_g and an electron affinity A_g with respect to the vacuum level E_{vac}. However, as a result of measuring these energies, e.g. by photoelectron spectroscopy or inverse photoelectron spectroscopy, the molecule becomes ionized. Thus, the ionization energy (HOMO) is measured by releasing an electron into the vacuum level, leaving a positively charged molecule (M^+), whereas the electron affinity (LUMO) is detected by capturing an electron from the vacuum level, resulting in a negatively charged molecule (M^-). In both cases, the final state is an ionized molecule where the configuration of the energy levels are altered. Typically, the electron affinity decreases to $A_g(M^-)$ and the ionization potential to $I_g(M^-)$, if an electron is added to the molecule [15]. This is caused by the Coulomb interaction between the electrons which then redistribute on the molecule. In the same way, the energy of the levels decreases if an electron is removed, increasing the electron affinity to $A_g(M^+)$ and the ionization potential to $I_g(M^+)$. Thus, electron affinity and ionization potential rather describe a process (of ionization) than an actual state and one can generally define both quantities

$$A_g(M^0) = E(M^0 + e^-) - E(M^-) \quad \text{and} \quad I_g(M^0) = E(M^+ + e^-) - E(M^0) \tag{2.5}$$

by the difference in energy of the system before and after ionization.

Polarization energy The energy levels of a molecule in the gas phase differ from the energy levels of an organic solid in which charges are conducted. Extra charges are present as electrons on the LUMO levels or as holes on the HOMO levels of the molecules, resulting in the ionization of the molecule. As a consequence, the environment of a molecule is polarized and adjacent molecules redistribute their charges in order reach an energetically favorable configuration, releasing a polarization energy. To release an electron from a neutral molecule, less energy is needed since the residual ionized molecule gains an extra energy by polarizing its neighbors. However, releasing an electron from a negatively charged molecule leads to a neutral molecule, so that an additional energy is required to depolarize the environment. Therefore, the ionization potential decreases whereas the electron affinity increases in an organic solid. The effect resembles charged molecules in solvents where the polarization of the environment similarly shifts the energy levels [15].

The polarization energies for holes

$$P_h = I_g - I_c' \tag{2.6}$$

are defined as the difference between the ionization potential of an organic crystal I_c' and a neutral molecule in gas phase. Analogously, the polarization energy for electrons

$$P_e = A_c' - A_g \tag{2.7}$$

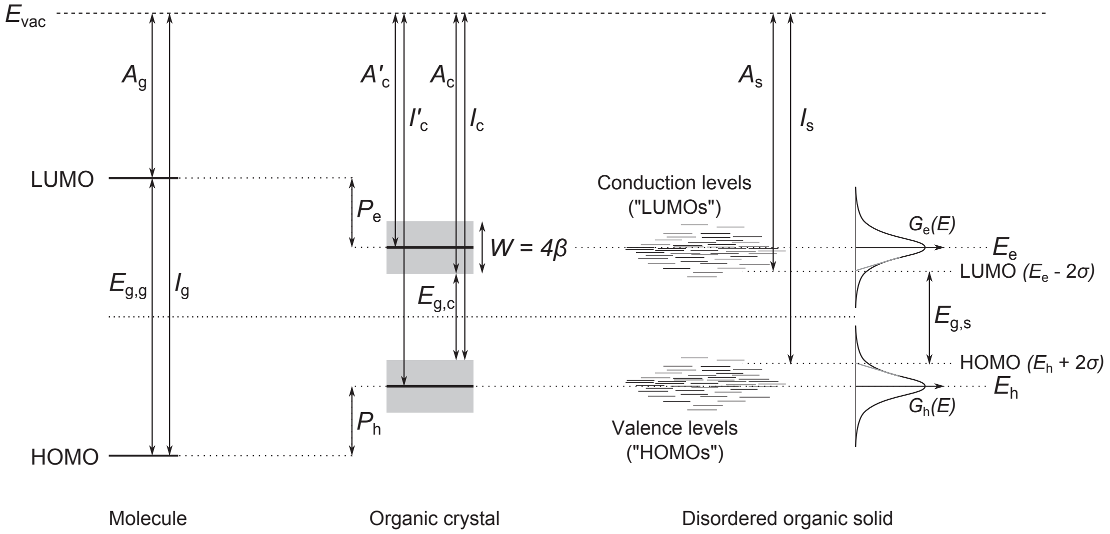

Figure 2.5: Energy diagram of a single neutral molecule (g), an organic crystal (c), and a disordered organic solid (s). Electron affinities (A_{g},A_{c},A_{s}) denote the position of the LUMO levels to the vacuum level whereas the ionization potentials (I_{g},I_{c},I_{s}) indicate the position of the HOMO to the vacuum level. In case of an organic crystal, the LUMO and the HOMO levels change to band-like states. Disordered organic solids show a Gaussian distribution of states $G_{\mathrm{e}}(E)$ and $G_{\mathrm{h}}(E)$ due to local variations in polarization energy P_{e} and P_{h}.

is defined by the difference of the corresponding electron affinities. Please note that I'_{c} and A'_{c} are given with respect to the center position of the distribution of states of a crystal or a disordered organic solid. In the first approximation, P_{e} and P_{h} are determined by calculating the interaction of the excess charge of the molecule with the dipoles of the molecules in the crystal. Then, P_{e} and P_{h} are equally given by

$$P_{\mathrm{e}} = P_{\mathrm{h}} \propto \sum_{k=1}^{N-1} \frac{e^2 \bar{\alpha}_{\mathrm{p}}}{2 r_k^4} \tag{2.8}$$

because the isotropic mean polarizability $\bar{\alpha}_{\mathrm{p}}$ does not depend on whether the molecule is charged positively or negatively. Here, r_k is the distance between the center of the charged molecule and molecule of the crystal indexed by k [16]. Typical polarization energies are in the range of 1 eV, leading to energy states in the crystal which are closer to each other than given by the energy gap $E_{\mathrm{g,g}} = I_{\mathrm{g}} - A_{\mathrm{g}}$ of a single molecule [16].

Polarons In an ideal organic crystal, the polarization process can be explained by the following subprocesses. First of all, there is already a polarization because of the induced dipoles on each molecule, initiated by spontaneous polarization of one molecule. Releasing or capturing an electron on the molecule automatically changes the binding energy between two molecules and thus the polarization energy. However, polarization energies arising from the ionization of a molecule are much stronger. If a molecule is charged, negatively or positively, the surrounding molecules show an electronic polarization by redistributing their charges in order to form dipoles which minimize their energy in the Coulomb field of the ionized molecule (electronic relaxation) [16]. This process is much faster than the transition of a charge carrier from one molecule to an adjacent one, so that the energy of each charge carrier in an organic crystal is instantaneously influenced by the polarization of the environment. This phenomenon can be described by a quasi-particle called polaron, combining the excess charge of the molecule and its polarized environment to a single entity. The polaron further influences the lattice of the organic crystal by a vibronic relaxation [16]. In a first step, polarized molecules might show an intramolecular relaxation, leading to changes of shape and orientation. Second, polarized molecules are attracted towards the ionized molecules which locally changes the lattice constant in case of an organic crystal. Even though vibronic relaxation contributes to the polarization energy, the largest part is given by electronic relaxation.

For the distribution of states, one has to distinguish between two extrema. In the case of an ideal organic crystal, having a perfect periodicity, band-like states are observed, whereas in disordered organic solids energy states can be described as a broad distribution of localized states. However, several organic materials show a nano- or polycrystalline structure so that a mixture of both descriptions might apply.

Energy bands Given by the molecular orbitals, electrons are localized at the molecule. However, if molecules come close to each other, e.g. in a crystal, their wavefunctions start to overlap. As a consequence, the energy levels split around the energies of the initial molecular states. The resulting band structure can be obtained from tight-binding calculations, considering a periodicity of the solid potential

$$V(\vec{r}) = \sum_i V_i(\vec{r} - \vec{r}_i) \tag{2.9}$$

given by the sum over all single molecular potentials V_i. For this potential, the one-electron Schrödinger equation

$$\left(-\frac{\hbar^2\nabla^2}{2m} + V(\vec{r})\right)\psi_{\vec{k}}(\vec{r}) = E(\vec{k})\psi_{\vec{k}}(\vec{r}) \tag{2.10}$$

has to be solved which is justified for low charge carrier concentration and weak electron-electron interaction. Bloch found that it is possible to describe the resulting quantum-mechanical wavefunctions

$$\psi_{\vec{k}}(\vec{r} + \vec{R}) = \exp(i\vec{k}\cdot\vec{R})\psi_{\vec{k}}(\vec{r}) \tag{2.11}$$

such that they are invariant to translations by $\vec{R}$ being any multiple of the lattice vectors. As a consequence, they can be characterized by a single wavevector $\vec{k}$ with the absolute value $k = 2\pi/\lambda$ where λ is the spatial periodicity. These solutions of Eq. 2.11 are called Bloch waves, showing an energy dispersion for electrons of the form

$$\epsilon_\mathrm{e}(k_\mathrm{x}) = E_\mathrm{e} - 2\beta\cos(k_\mathrm{x}a) \tag{2.12}$$

for the one-dimensional case with the lattice constant a [15]. E_e is the center of the conduction band, depending on the polarization energy of the molecules in the organic crystal and β is the energy of interaction between neighboring molecules, resulting from their transfer integral in analogy to Eq. 2.1. Such a calculation can be applied to any molecular orbital, but it is mainly relevant for the electrons of the delocalized π orbitals in their outer shell. Thus, a conduction band forms for excess electrons and a valence band for excess holes, as visualized in Fig. 2.5. The width of the band is $W = 4\beta$, which for crystals is in the range of several 100 meV (cf. Fig. 2.5)

[16]. It becomes the larger the more the wavefunctions of the molecules overlap. For instance, the prototypical organic crystal showing band structures, anthracene, has a bandwidth of ca. 500 meV for both, the conduction and the valence band. Pentacene, a commonly used hole conducting material has a valence bandwidth of 740 meV [27]. The energy band gap between the valence band and the conduction band is defined by their electron affinity and ionization potential as

$$E_{g,c} = I_c - A_c \tag{2.13}$$

indicated in Fig. 2.5. One should note here that calculated energy band widths are only valid for low temperatures close to $T = 0\,\mathrm{K}$. At larger temperatures, interactions with phonons increase, reducing the scattering time as well as the mean free path, so that charges become increasingly localized, which effectively minimizes the band width.

More sophisticated band structures can be achieved by considering the interaction of the electron with the lattice of the crystal. Each electron displaces the molecules in its environment due to the polarization effect. This can be involved e.g. by considering polaron-like transport [15, 27, 28]. However, band transport does not play a role for the organic materials used in this work so that band structure is treated here only rudimentarily.

Disordered organic solids Organic devices commonly consist molecular solids showing energetic disorder. Instead of delocalized electron waves, charge is localized on each molecule. Since a translational symmetry does not exist, each molecule has a different environment and surrounding molecules differ in their orientation and distance. As a consequence, the polarization energy calculated by Eq. 2.8 differs for each molecule by a value of ΔP_e for a negative ionized molecule and ΔP_h for a positive charged molecule from the mean value P_e and P_h [16]. As argued above, $P_e = P_h$, and it can be assumed that $\Delta P_e = \Delta P_h$ applies likewise. Furthermore, the positional disorder of the molecules leads to variations in the overlap of the molecular orbitals and the related splitting of the energy states also fluctuates in dependence of the coupling, e.g. expressed by the transfer integral.

As depicted in Fig. 2.5, the LUMO and the HOMO levels of all molecules form a set of localized conduction and valence levels in the solid, often referred to as "LUMOs" and "HOMOs". One can show by photoelectron spectroscopy and by absorption spectra that these states follow a Gaussian distribution of states (Gaussian DOS)

$$G_{e/h}(E) = \frac{N_{e/h}}{\sqrt{2\pi}\sigma_{e/h}} \exp\left[-\frac{(E - E_{e/h})^2}{2\sigma_{e/h}^2}\right] \tag{2.14}$$

where $N_{e/h}$ are the number of states associated with the number of molecules per volume unit cell, but can be larger if the molecular state is degenerate. $E_{e/h}$ are the energies of the center positions and $\sigma_{e/h}$ are the Gaussian widths of the distributions. $\sigma_{e/h}$ is different for each type of molecular material, typically in the range from 4 to 6 $k_B T_0$ ($\sim$100-150 meV) [29].

The variation in energy depends on several aspects: First, on the degree of disorder itself, i.e. the ratio between regular and irregular arrangements of molecules. Second, as given in Eq. 2.8, the polarization energy depends linearly on the isotropic polarizability of the molecules, so that its variation is more pronounced in a medium which can be easily polarized or is already polar [21]. Third, the inverse of the fourth power of the distance between the molecules goes into the polarization energy. Thus, fluctuations of the intermolecular distance increase the energetic disorder. However, this contribution is weakened by the fact that each molecule has several neighbors, so that fluctuations are averaged, but it might be more pronounced if local fluctuations of the packing density occur.

In the case of molecules, the ionization potential and electron affinity are well-defined. However, for a Gaussian DOS, abrupt energetic limits are not given. Therefore, meaningful onset energies have to be defined. This is typically done by defining the electron affinity of a Gaussian disordered organic solid at

$$A_\mathrm{s} = E_\mathrm{e} - 2\sigma \tag{2.15}$$

and the ionization potential as

$$I_\mathrm{s} = E_\mathrm{h} + 2\sigma\,. \tag{2.16}$$

Often the wording "LUMO" and "HOMO" of an organic semiconductor is used to describe the onset of the conduction and the valence levels, respectively. It depends on the context whether they designate properties of a single organic molecule or an organic semiconductor. Graphically, these points can be interpreted as the linear extrapolation of the tangent at the Gaussian's turning point towards zero, directing to the energy gap [30]. Thus, the onset energies are identified with a substantial rise of the density of the states per unit energy. Below the onset energy lie only 2.3% of the total density of states $N_\mathrm{e/h}$. However, this can be a large amount of charge carriers if these states are filled. For example, an electron concentration of $2.3 \times 10^{19}\,\mathrm{cm}^{-3}$ would be achieved for $N_\mathrm{e} = 10^{21}\,\mathrm{cm}^{-3}$. The width of the Gaussian distribution can be characterized by 4σ in which 95.5% of all states lie. For energetic disorder σ between 100 meV to 150 meV, a width 4σ in the range of 400 meV to 600 meV is found, comparable to the bandwidth in organic crystals.

Occupation of energy states Energy states, given by the band structure or by the Gaussian DOS, are filled by electrons according to the Fermi-Dirac statistics

$$F(E) = \frac{1}{1 + \exp\left[\frac{E - E_\mathrm{F}}{k_\mathrm{B} T}\right]} \tag{2.17}$$

and thus are in agreement with the Pauli principle that fermions have to differ in their quantum states if they share the same position. E_F is the Fermi energy level, and together with the temperature T, it defines the occupation of the states. For energies $E \ll E_\mathrm{F}$, the occupation probability is one and the corresponding states are permanently filled. If $E - E_\mathrm{F} \gg k_\mathrm{B} T$, the probability that a state is occupied by an electron decreases exponentially. The Fermi level corresponds to the energy at which a state has a probability of 50% to be occupied. Further, charge neutrality must be fulfilled: $n = p$. Simply spoken, the total number of free electrons n above the Fermi level must equal the total number of free holes p below the Fermi level. As a consequence, the Fermi level is not fixed but can change its position with temperature, e.g. due to releasing or capturing of charges by impurity levels. In the case of an intrinsic semiconductor, the Fermi level aligns at the midgap position between the conduction band and the valence band or their equivalent Gaussian distribution of levels provided that the density of states is symmetric in energy and equally degenerated.

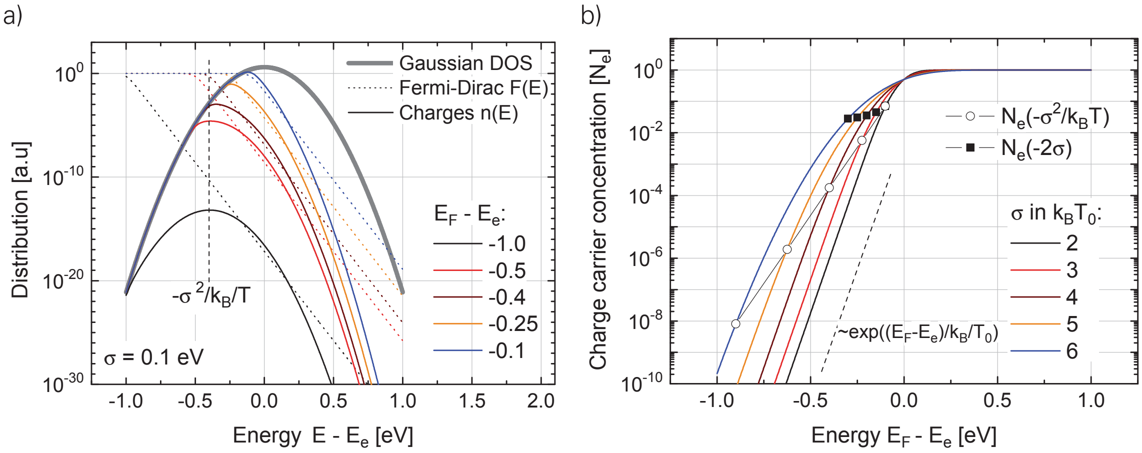

Figure 2.6: a) Comparison of the charge distribution n(E) for different Fermi levels in a Gaussian DOS at room temperature T_0. For comparison, the Fermi-Dirac statistics is visualized by dotted lines and the Gaussian is normalized to one. b) Charge carrier concentration vs. Fermi level position with respect to the center position of the Gaussian. Extra symbols indicate the charge carrier concentration at the equilibrium level ($-\sigma^2/k_BT$) and the onset energy (-2σ) for various values of σ. The charge concentration at which the Fermi level exceeds the equilibrium level is much lower for conduction levels with a higher energetic disorder. For a Fermi level close to the onset energy, very high charge carrier concentrations are already achieved.

In Fig. 2.6a), the Fermi-Dirac statistics for electrons (dotted lines) are shown for various Fermi levels with respect to the center E_e of the Gaussian DOS for electrons. Energies are defined similar to Fig. 2.5 to be increasing towards the vacuum level. For larger positive energies, the straight lines clearly indicate an exponential law, so that the Boltzmann approximation $F(E) \propto \exp(-(E-E_F)/k_BT)$ can be used. For an energetic disorder of $\sigma = 0.1$ eV, the Gaussian DOS is also plotted. The number of charges per state, called the occupied DOS (ODOS)

$$n(E) = G(E)F(E) \tag{2.18}$$

can be determined by multiplying the DOS with the distribution function. This applies equally for band structures or disordered states. Here, the situation will be discussed for a Gaussian DOS which commonly represents organic semiconductors as used in OLEDs, organic solar cells, or other devices as investigated in this work, where materials have mobilities of 1 $\mathrm{cm^2/Vs}$ or lower. Furthermore, the interplay between a Gaussian and a Fermi-Dirac statistics leads to an interesting behavior which is special for organic semiconductors and distinguishes them from inorganic semiconductors. For that reason, the function $n(E)$ is presented for various Fermi levels in Fig. 2.6a). If the Fermi level is far away from the center of Gaussian DOS, one can show that most of the charges are located at the equilibrium level

$$E_\infty = E_e - \frac{\sigma^2}{k_BT} \tag{2.19}$$

to which charges on average relax for $t \to \infty$ if they start from a non-equilibrium distribution. Interestingly, this level is independent from the position of the Fermi level itself even though the number of charges might vary [21]. The result can be understood by considering the fact that the Fermi-Dirac statistics decreases exponentially, while the number of states basically increases with the square of an exponential law and thus much stronger. In this regime, the total number of free charge carriers

$$n = \int_{-\infty}^{\infty} n(E)dE \tag{2.20}$$

increases exponentially with the shift of the Fermi level. This can be seen in Fig. 2.6b) by a nearly straight increase in the semi-logarithmic plot of the charge carrier density vs. the Fermi level position. Charge carrier densities are given there in units of the total number of states

$$N_\mathrm{e} = \int_{-\infty}^{\infty} G(E)dE \tag{2.21}$$

as determined by the Gaussian DOS in Eq. 2.14. The situation changes if the Fermi level crosses the equilibrium level and now the maximum of the charge distribution $n(E)$ shift towards the vacuum level (cf. Fig. 2.6a). Since the equilibrium level depends on the energetic disorder σ of the Gaussian DOS, properties of an organic semiconductor are strongly correlated to the spread of the LUMOs and HOMOs. In Fig. 2.6b), the charge carrier density where the Fermi level equals the equilibrium level is indicated by open circles for various values of σ. It is seen that for smaller σ, the charge carrier concentration has to be much larger until electrons are able to effectively occupy higher levels in the Gaussian DOS. In contrast, the charge carrier density where the Fermi level equals the LUMO onset (filled circles) is extremely high, reaching values only obtained for organic field-effect transistors in strong charge accumulation (cf. Sec. 3.1). Thus, most relevant for organic semiconductors is the range of energy levels spanning from the equilibrium level to the onset level. The energy levels closer to the center of the Gaussian DOS are indeed more frequent, but also more seldom occupied. If the Fermi level further shifts to the center of the distribution of states, half of all states are filled, independent from the energetic disorder. The charge carrier concentration finally converges to N_e where all states are occupied for a further decrease of the Fermi level energy. It will be shown in the next section that this kind of state filling directly influences the description of charge transport in disordered organic semiconductors.

Trap states Besides the conduction levels or the valence levels, trap levels might exist in the energy gap. One can assume that their concentration is orders of magnitude smaller than the total number of states per volume cell $N_\mathrm{e/h}$, so that they can be treated as additional energy states. However, even an extremely low amount of trap states in the range of $N_\mathrm{t} = 10^{16}\,\mathrm{cm}^{-3}$ can have a substantial influence onto charge transport properties. Like any other energy state, they are filled if they are below the Fermi level. One distinguishes between shallow and deep traps. The former are closer to the LUMO or to the HOMO of an organic semiconductor and trapped charges can even be released at room temperature. Deep traps are closer to the midgap position where trapped charges need a substantial amount of energy to be released [16]. Traps have mainly two effects: They capture charges and thus decrease the amount of free charge carriers which can take part in the charge transport. As a result, the electric conductivity drops. Besides that, trapped charges influence the electric field within an organic semiconductor layer. Due to

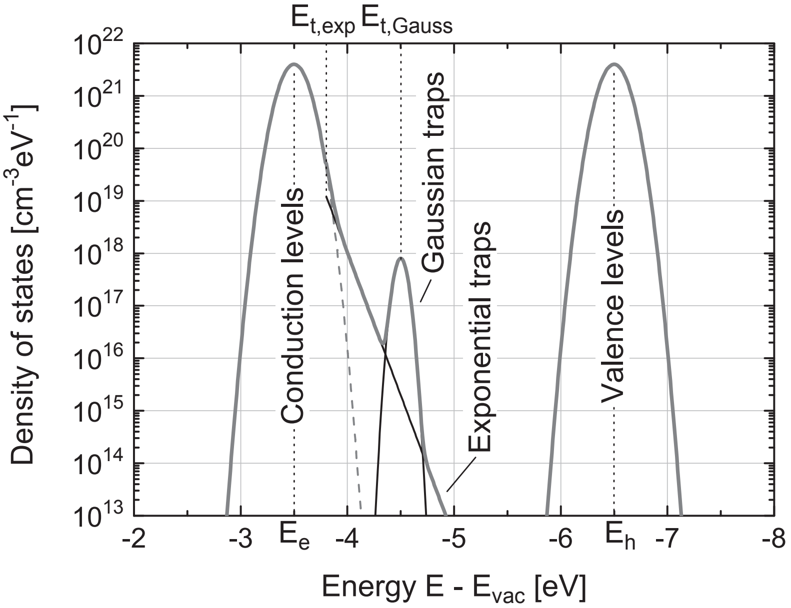

Figure 2.7: Density of states for a disordered organic semiconductor including trap states with Gaussian DOS. Additionally, trap states can occur with an exponential or Gaussian distribution. The sum of all distributions is indicated by a thick gray line. Depending on the energy range, different traps states can be dominant. Parameters are: $E_e = -3.5\,\text{eV}$, $E_h = -6.5\,\text{eV}$, $N_{e/h} = 10^{21}\,\text{cm}^{-3}$, $\sigma_{e/h} = 0.1\,\text{eV}$, $E_{t,0} = -3.8\,\text{eV}$, $E_{t,dec} = 0.08\,\text{eV}$, $N_{t,exp} = 10^{18}\,\text{cm}^{-3}$, $E_{t,gauss} = -4.5\,\text{eV}$, $\sigma_t = 0.05\,\text{eV}$, $N_{t,gauss} = 10^{17}\,\text{cm}^{-3}$.

Coulomb interaction, charges of the same polarity of the trapped one are repulsed, hindering the charge transport. Thus, traps affect the properties of an organic semiconductor in a negative manner, and the intention is to avoid them.

Several origins for trap states can be mentioned: Structural defects within the crystal lattice can trap charges. In a disordered organic solid, morphological configurations might exist which lead to extreme polarization energies, so that strongly outlying conduction or valence levels of the Gaussian DOS act as trap states. Further, the organic material can be contaminated by other substances and molecules, so that materials have to be highly purified by subliming them several times in order to avoid trap states [31]. However, if the organic semiconductor is doped by other donor or acceptor molecules, as discussed in Sec. 2.2.2, these molecules are ionized and then could act as a charge trap. Trap formation is also discussed under the aspect of long-term stability of organic devices under ambient conditions. Some organic molecules degrade by reacting with oxygen or water, and the reaction products might have energy levels within the gap. Even if a chemical reaction does not take place, air components can be physically adsorbed within the organic solid, resulting in trap states, e.g. by a polarization energy shift of the molecules, or by influencing the molecular orbitals.

Traps states are often described in literature by a Gaussian distribution of states

$$G_{\text{t, Gauss}} = \frac{N_{\text{t,gauss}}}{\sqrt{2\pi}\sigma_{\text{t}}} \exp\left(\frac{(E - E_{\text{t,gauss}})^2}{2\sigma_{\text{t}}^2}\right) \tag{2.22}$$

where $N_{\mathrm{t,gauss}}$ is the density of trap states, σ_{t} their energetic disorder, and $E_{\mathrm{t,gauss}}$ defines the energy of the center position. Alternatively, an exponential distribution

$$G_{\mathrm{t,\ exp}} = \frac{N_{\mathrm{t,exp}}}{E_{\mathrm{t,dec}}} \exp\left(-\frac{E - E_{\mathrm{t,exp}}}{E_{\mathrm{t,dec}}}\right) \tag{2.23}$$

is used for energies $E \geq E_{\mathrm{t,exp}}$. Here, $N_{\mathrm{t,exp}}$ is the density of trap states and $E_{\mathrm{t,dec}}$ a decay energy coefficient [15]. The total distribution of trap states can then be assembled by considering a superposition of several trap types and their distributions [32]. In Fig. 2.7, an example is given for an exponential and a Gaussian distribution of trap states, forming traps between the conduction and the valence levels for parameters given in the figure caption. An exponential distribution is typically used when the number of trap states decays from energies e.g of the LUMOs or HOMOs into the energy gap whereas a Gaussian distribution can be applied to describe a trap level with a rather discrete energy.

2.1.4 Charge transport

Charge carrier mobility If an electric field F is applied to an isotropic medium with a homogeneous charge carrier concentration n, a current flow

$$j = \sigma F = qnv_{\mathrm{D}} \tag{2.24}$$

is obtained, characterized by the conductivity σ. One can interpret this current density j as the motion of charges through the medium with a mean drift velocity v_{D}. The charge transport process itself is described by the charge carrier mobility μ defined by

$$v_{\mathrm{D}} = \mu F \tag{2.25}$$

and the conductivity of the medium reads then

$$\sigma = qn\mu\,. \tag{2.26}$$

A first interpretation of the mobility was given by Paul Drude. He described the motion of electrons as free, so that their acceleration in the electrical field is undisturbed, but considered that charge carriers are fully slowed down by collisions with the lattice ions [16]. The mean relaxation time τ between two collisions is then related to the charge carrier mobility by

$$\mu = \frac{q\tau}{m} \tag{2.27}$$

where m is the electron mass. With that model, the reduction of the mobility in metals with increasing temperature has been explained: Lattice vibration become stronger at higher temperatures, increasing the probability for collisions with ions which in turn decreases the mean relaxation time τ. A drawback of the Drude model is the reduction of the mobility to a mean relaxation time, an effective value which still has to be related to a physical process. Furthermore, the model is unsuitable if charges cannot be considered as free, like in the case of amorphous organic semiconductors or insulators. Then, the mean relaxation time has to be understood as a time constant characterizing on which time scale charge momentum relaxation takes place. However, in the case of band-like transport in semiconductors, the Drude model can be modified in order to predict the charge carrier mobilities depending on the scattering processes occurring.

Band transport Band transport has been obtained in highly crystalline organic materials or single crystals [33]. Then, charges are fully delocalized over the lattice described by the energy band structure $\epsilon(k)$. At zero electrical field, the current density associated with the momentum of all electrons adds to zero because of $\epsilon(k) = \epsilon(-k)$ and because the deepest levels are symmetrically filled. If an electrical field is applied, charges accelerate by occupying states with higher momentum k and energy ϵ of the energy band structure. This process cannot be described like for a free electron since an interaction with the lattice takes place which make the charge carrier behave as having an effective mass m^* [33]. This mass can be deduced from the energy band structure by

$$\frac{1}{m^*} = \frac{1}{\hbar^2}\frac{d^2\epsilon}{dk^2} \tag{2.28}$$

locally approximating a parabolic shape of $\epsilon(k)$. Further, only electrons close to the Fermi energy are of interest because charges with lower energy cancel each other regarding the transport of charge as discussed above. Accordingly, the Drude model can be changed to

$$\mu = \frac{q\,\tau(E_\mathrm{F})}{m^*} \tag{2.29}$$

where the mass of a free electron is replaced by the effective mass, and the mean relaxation time is evaluated for charges at the Fermi energy. It can be assumed that the mobility is larger the larger the bandwidth is. In that case, the effective mass will be lower for a cos(ka)-like energy dispersion (cf. Eq. 2.12). This can be understood, when one considers that a larger bandwidth is related to an increased energy of the transfer integral between neighboring molecules.

Since the effective mass is defined by the energy band structure and thus determined by the overlap of the molecular orbitals, the mobility found for band transport is finally limited by scattering processes. At room temperature, scattering with phonons, which reduces with decreasing temperature, affects the charge transport and a $\mu \propto T^{-3/2}$ law applies. In general, increasing mobilities at decreasing temperature are a strong indicator for band transport. However, for these organic semiconductors, the temperature dependence of the mobility deviates from an ideal T^n law with $n = -3/2$, rather leading to estimated values of n between 0 and -3 [16]. It is expected that the purity and degree of crystallinity plays a major role. At very low temperatures, the relation is reverse because Rutherford scattering at ionized traps becomes dominant and a $\mu \propto T^{3/2}$ law applies as seen for conventional inorganic semiconductors. Organic semiconductors do not necessarily show this behavior at low temperatures (T<50 K) because a saturation in mobility might occur. As possible explanations, the onset of optical phonon emission due to electron scattering as well as an increase of effective mass near the surface of the Brillouin zone are discussed [33].

There are some requirements for band-like charge transport. The quantum-mechanical uncertainty relation between energy and time must be fulfilled. A charge carrier is determined in energy by the width of the energy band W and in time by the mean relaxation time τ. Thus, $\tau \gg \hbar/W$ must apply [16]. Further, position and momentum must follow their uncertainty relation. The momentum is limited to $2\pi/a$ (with a being the lattice constant) because larger momentum than π/a provide the same result as wavevectors reduced to the interval $[-\pi/a, \pi/a]$ by multiples of $2\pi/a$. Thus, the uncertainty in position associated with the mean free length of the charge carrier must be much larger than the lattice constant: $\lambda >> a$ [16]. It can be assumed that these criteria are only met by organic semiconductors which reach mobilities in the range of 1 to 10 cm^2/Vs [21]. Conversely, one can assume that extremely high mobilities are only reached if organic materials show a high degree of crystallinity. For example, highly purified naphthalene reaches charge carrier mobilities up to 400 cm^2/Vs at very low temperatures (10 K) and high electric field [33]. At room temperature, measured mobilities for various materials are in the range of 1 cm^2/Vs, still showing an increase of mobility with decreasing temperature [16]. Measured mobilities depend on the type of charge carrier, electron or hole, and on the crystal direction in which the current flows. Due to the anisotropy in shape of the most molecules and the orientation of the molecular orbitals, the crystal lattice is also anisotropic, affecting the mobility. However, variations are typically within one order of magnitude [16].

Hopping transport In an amorphous organic semiconductor, the energy states show energetic and spatial disorder as described by Eq. 2.4 and 2.14. Figure 2.8 schematically visualizes the Gaussian DOS. Charge carriers are localized on a molecule and move by incoherent hopping transport from one site i to the next j. Due to the overlap of the electronic wave functions of nearby molecules, electrons do not overcome the whole potential barrier, but rather tunnel. However, the energies of the molecular states have to match, so that inelastic scattering with phonons is required and necessarily incorporated with the loss of coherence. One can associate then the corresponding transition rates ν_{ij} with a phonon-induced tunneling process as described by Miller-Abrahams rates [34]:

$$\nu_{ij} = \nu_0 \exp\left(-2\gamma r_{ij}\right) \begin{cases} \exp\left(-\frac{\epsilon_j - \epsilon_i}{k_\mathrm{B} T}\right) & , \quad \epsilon_j > \epsilon_i \\ 1 & , \quad \epsilon_j \leq \epsilon_i \, . \end{cases} \tag{2.30}$$

The activation energy is given by the energy difference $\epsilon_j - \epsilon_i$ between two molecule sites i and j and the distance r_{ij} between two molecules determines the tunneling probability. Here, γ is defined as introduced by Eq. 2.4, being the inverse localization radius and the prefactor ν_0 is a constant rate, being the upper limit of the hopping rates [21]. Transitions to energy states with lower energy are preferred whereas transitions to states with higher energies become unlikely for $\epsilon_j - \epsilon_i \gg k_\mathrm{B} T$. Such a description is used in the Gaussian disorder model (GDM) developed for simulation of transport of nearest neighbor hopping in a cubic lattice with molecule sites of energies following the Gaussian DOS of an organic semiconductor. Alternatively to Miller-Abrahams rates, Marcus theory yields rates, calculated by quantum-chemical procedures:

$$\nu_{ij} \propto \frac{J_0}{\sqrt{\lambda}} \exp\left(-\frac{\lambda}{4 k_\mathrm{B} T}\right) \exp\left(-\frac{(\epsilon_j - \epsilon_i)^2}{4 \lambda k_\mathrm{B} T}\right) \tag{2.31}$$

where J_0 is the transfer integral and λ is the reorganization energy [35–37]. However, the qualitative results remain unchanged, so that here the GDM is presented in order to explain the basic physics of hopping transport [37].

Effective charge transport can take place if a charge carrier gradient exists or an external electric field F is applied. The latter scenario is shown in Fig. 2.8. There, the electric field introduces a spatially increasing energy shift of the conduction levels. Hopping downwards has always the same probability, but upwards jumps along the direction of the electric field become more probable because electrons gain an energy of ca. $e|F|a$, with a the mean distance of the molecules. Simultaneously, jumps against the direction of the electric field become more unlikely. Consequently, charges are effectively transported by the electric field due to an asymmetry of the average hopping rates in both directions. Figure 2.8 exemplarily shows the motion of a single electron. Larger distances can only be covered if both, downward and upward jumps, are performed. On average, a charge carrier has then a higher energy as at the equilibrium level which can be associated with a transport level E_{tr}. The position of the transport level can be understood as a compromise between mandatory upwards jumps with low rates and preferred downward jumps with comparably fast rates. A consistent definition of the transport level, however, is not given in literature, because it is unclear which properties and dependencies the transport level should have. An overview about various definitions can be found elsewhere [38, p. 32f].

In contrast to Fig. 2.8, hopping transport has to be understood as a three-dimensional process. In a one-dimensional chain of sites, the transition with the lowest transition rate would determine the whole charge transport. However, in three dimensions, charge carriers take mainly paths through the organic semiconductor in agreement with the transport level. Thus, molecules with higher energies can be bypassed by a larger travel distance. For example, Sharma *et al.* found that this is important for charge transport in organic field-effect transistors, especially at high energetic disorder [39].

Two relevant regimes exist for hopping transport: low and high charge carrier concentration. If the Fermi level is below the equilibrium energy, most of the charges have energies around E_∞, independent from the Fermi level. This regimes ends at a charge carrier concentration, depending strongly on the energetic disorder as outlined by Fig.2.6b). In the second case, the Fermi level exceeds the equilibrium level and the electrons are able to occupy higher energy levels.

Low charge carrier concentration Applying the GDM, Bässler has investigated hopping transport by Monte Carlo simulations at a low charge concentration [22]. The main outcome is a temperature-dependent mobility

$$\mu(T) = \mu_0 \exp\left(-\frac{4}{9}\hat{\sigma}^2\right) \tag{2.32}$$

where μ_0 is the mobility for $F = 0$ and $\hat{\sigma} = \sigma/k_\mathrm{B}T$. The typical $\ln\mu \propto T^{-2}$ law for a low charge carrier concentration can be explained by the activation of the charge carriers from the equilibrium level to the transport level, corresponding to $\exp\left(-(E_{\mathrm{tr}} - E_\infty)/k_\mathrm{B}T\right)$. Because the position of the equilibrium level is also associated with the temperature by $E_\infty = E_\mathrm{e} + \sigma^2/k_\mathrm{B}T$, one ends up with a quadratic temperature dependence in the denominator of the exponent. Under this assumption, the transport level can be denoted by

$$E_{\mathrm{tr}} = E_\mathrm{e} - \frac{5}{9}\frac{\sigma^2}{k_\mathrm{B}T} \tag{2.33}$$

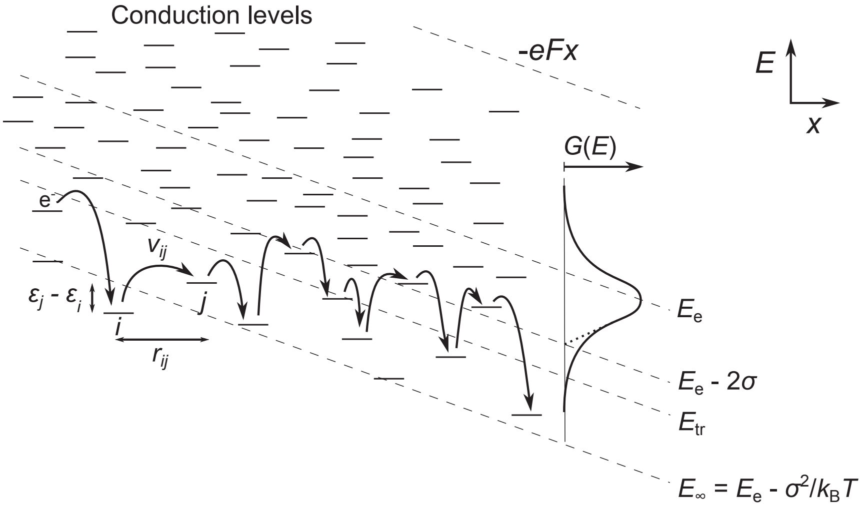

Figure 2.8: Charge transport in an amorphous organic solid with a Gaussian DOS. Charge carriers move by hopping from one site to another. The hopping rate ν_{ij} is mainly determined by the energy $\epsilon_j - \epsilon_i$ and the distance r_{ij} between the molecular sites j and i. By applying an electric field F, the center position of the Gaussian DOS E_e is locally shifted and with that the energy of the transport level E_{tr}. This energy can be seen as an average energy a charge carrier has if transported by hopping. Figure follows Ref. [16, p. 261]

and lies approximately in the middle between E_e and E_∞.

Further evaluations regarding spatial disorder eventually resulted in the empirical formula

$$\mu(\hat{\sigma}, F) = \mu_0 \exp\left(-\frac{4}{9}\hat{\sigma}^2\right) \exp\left[C\left(\hat{\sigma}^2 - 2.25\right)\sqrt{F}\right] \quad , \quad \Sigma \geq 1.5 \tag{2.34}$$

$$\mu(\hat{\sigma}, F) = \mu_0 \exp\left(-\frac{4}{9}\hat{\sigma}^2\right) \exp\left[C\left(\hat{\sigma}^2 - \Sigma^2\right)\sqrt{F}\right] \quad , \quad \Sigma \leq 1.5 \tag{2.35}$$

which fits the outcome of the Monte Carlo simulations. It can be seen that Eq. 2.32 is extended by a second exponential term, considering the spatial disorder parameter Σ (cf. Eq. 2.4) and an electric field dependence which is similar to a Poole-Frenkel law $\ln\mu \propto \sqrt{F}$ as a natural outcome of the GDM [21,40]. Such a field dependence basically is usually found if the potential of a defect state is superimposed by a Coulomb potential due to image-forces. The energy barrier noticeably decreases for releasing a charge carrier if an electric field is applied, similar to the effect of image-force induced Schottky-barrier lowering at injection contacts, as discussed in Sec. 2.2.2. For low spatial disorder, the effect on the field dependence is negligible. However, for $\Sigma \geq 1.5$, a negative field dependence is introduced which can become dominant for $\Sigma > \hat{\sigma}$, so that the mobility decreases with increasing field. In this case, the spatial disorder is larger than the energetic disorder and it is likely that charges even flow against the direction of the electric field in order to overcome energy barriers introduced by molecules with higher energies. With the increase of the electric field, charge transport against the electric field becomes unlikely and charge carriers are locally trapped by molecules introducing large energy barriers which reduces the mobility [21,41]. Thus, the GDM shows a dependence of mobility on temperature and electric field, but a dependence on the charge carrier concentration is neglected. This is related to the fixed position of the equilibrium level, so that at low charge carrier concentrations the energetic distance to the transport level remains constant for the charge carriers.

High charge carrier concentration The situation changes if the charge carrier concentration strongly increases, characterized by a shift of the Fermi level beyond the equilibrium energy. The corresponding charge carrier concentration related to this transition strongly depends on the energetic disorder of the molecular sites as shown in Fig. 2.6b) whereas spatial disorder does not have an effect [21]. Then, the dependence of the mobility on temperature and electric field change. Furthermore, an additional dependence on the charge carrier concentration is introduced. The effect has been experimentally shown by Tanase *et al.* who demonstrated a change in mobility by three orders of magnitude with the increase of charge carrier concentration by comparing charge flow in diodes and organic field-effect transistors. The GDM is not able to describe this effect because the Coulomb interaction is not modeled and only a single charge carrier in an empty lattice of sites is considered. Pasveer *et al.* investigated higher charge carrier concentrations by numerically solving the master equation

$$\sum_{j \neq i} \left(\nu_{ij} p_{\mathrm{i}} (1 - p_j) - \nu_{ji} p_j (1 - p_i) \right) = 0 \tag{2.36}$$

for the steady state in a mean-field approximation. [42]. Here, p_i is the occupation probability of the site i. Interestingly, the factor $(1 - p_i)$ accounts for Coulomb interaction and makes a multiple occupation of sites unlikely. Charges are now forced to stay at higher energy sites, e.g. above the equilibrium level at higher charge carrier concentration. The result of the so called extended Gaussian disorder model (EGDM) is parametrized by the equation

$$\mu(T, F, n) = \mu_0(T) g_1(F, T) g_2(n, T) \tag{2.37}$$

whereby $\mu_0(T)$ equals the original $\mu(T)$ of Eq. 2.32. The dependence on the electric field or the charge carrier concentration is separated into unit-free factors. The field dependence is given by

$$g_1(F, T) = \exp\left[0.44 (\hat{\sigma}^{3/2} - 2.2) \left(\sqrt{1 + 0.8 \left(\frac{Fea}{\sigma} \right)^2} - 1 \right) \right] \tag{2.38}$$

and the charger carrier concentration dependence follows

$$g_2(n, T) = \exp\left[\frac{1}{2} \left(\hat{\sigma}^2 - \hat{\sigma} \right) \left(2na^3 \right)^{\delta} \right] \tag{2.39}$$

with the lattice constant $a = N_{\mathrm{e}}^{-3}$ and $\delta = \frac{2}{\hat{\sigma}^2} \left[\ln\left(\hat{\sigma}^2 - \hat{\sigma} \right) - \ln(\ln 4) \right]$. In both cases, the variation with the field or the charge carrier concentration is more pronounced if the energetic disorder is large whereas for $\hat{\sigma} = 2$ both effects play a minor role. A further outcome is that the temperature dependence of the mobility is influenced by the charge carrier concentration. Whereas for low charge carrier concentrations, the typical $\ln \mu \propto T^{-2}$ law is found, it changes over to $\ln \mu \propto T^{-1}$ at high charge carrier concentration. Analytical treatments on the influence of a high charge carrier concentration yield qualitative similar results, confirming the picture of a mobility dependence $\mu = \mu(T, F, n)$ [36].

Spatial correlation of energetic disorder Based on the EGDM, analytical expressions are obtained for the mobility that can be used in ordinary drift-diffusion simulations. Fitted current-voltage curves of polymer based devices yielded a parameter set which describes the current flow over the measured range of temperatures and voltages. However, the parameters did not coincide with physical counterparts, e.g. the lattice constant is too large [42].

The GDM and the EGDM do not assume spatial correlation between the energies of the sites. This seems to be incorrect as argued by Gartstein and Conwell [43]. One can assume dipole moments located at each site which introduces a mutual interaction between them, shifting the polarization energy by the same value [44]. Furthermore, the interaction of charges with permanent dipoles is found to be a reason for spatial correlation [45]. Thus, for each molecule there exists a local correlation to its neighbors, decaying with the distance between two molecules. Typically, the correlation is already strongly reduced beyond 5 inter-site distances [43]. The spatial correlation of energy sites can be understood as a local smoothing or equalizing of the Gaussian disorder, so that it becomes easier for charge carriers to find a neighboring site of similar energy. In that sense, the larger lattice constant obtained by the EGDM model can be understood as an indication for spatial correlation in the investigated system. Another source for spatial correlation can be found for nanocrystalline organic materials. In each grain, there is a periodic lattice structure, so that fluctuations of the polarization energy are minimized and the energies of the sites are more equal. Then, it can be assumed that charge transport will proceed faster in the crystallites and grain boundaries become limiting due to stronger variation in site energies there. In principle, such a behavior could also be explained by assuming a larger lattice constant if spatial correlation is not considered.

The correlated disorder model (CDM) is in better agreement with the Poole-Frenkel law $\ln(\mu) \propto \sqrt{F}$ over a wider range of electric field [44, 45]. The original GDM showed deviations especially at low electric fields [21]. In order to realize a Gaussian DOS with spatial correlation of the energy sites, one can assume dipole moments d on each site with arbitrary orientation [46]. Now, site energies are given by

$$\epsilon_i = -\sum_{j \neq i} \frac{e d_j (\vec{r}_i - \vec{r}_j)}{\epsilon |\vec{r}_i - \vec{r}_j|^3} \tag{2.40}$$

as a sum over the dipole interaction of the molecule located at $\vec{r}_i$ with all other molecules located at $\vec{r}_j$. Bouhassoune *et al.* integrated this approach into the original EGDM [47]. The outcome of the corresponding extended correlated disorder model (ECDM) is compared with the EGDM and is summarized here. In the low field and low charge carrier concentration regime, the mobility dependence of the temperature is again given similar to Eq 2.32. However, the dependence of the mobility on the charge carrier concentration is less pronounced in the ECDM, but still shows a substantial increase of mobility with charge carrier concentration. In contrast to that, the field dependence is more distinctive and the ECDM accounts also for a reduction of the mobility at the highest field as already suggested by the GDM, but missing in the EGDM. Although both models are able to fit the same experimental data, the parameter sets obtained by the ECDM seem more realistic.

2.2 SEMICONDUCTOR STRUCTURES

2.2.1 Semiconductor statistics and transport

The previous section summarizes important properties of organic semiconductors. In this context, the mobility dependencies characterizing the charge transport as well as how the density of states fills with charge carriers are unique for molecular solids. Now, the focus changes from single molecules and their interaction with the local environment to molecular layers and their interaction with metallic electrodes and dielectric components in larger arrangements.

First of all, flow of electrons originates from either a gradient of the electric potential Φ

$$\vec{j}_{\mathrm{drift}} = qn\hat{\mu}\,\vec{\nabla}\Phi(\vec{r}) \tag{2.41}$$

or from a gradient of the charge carrier concentration n

$$\vec{j}_{\mathrm{diffusion}} = -q\hat{D}\,\vec{\nabla}n(\vec{r}) \tag{2.42}$$

which superimpose with each other. The direction of the drift current has not necessarily to coincide with the direction of the electric field $\vec{F} = -\vec{\nabla}\Phi$. The reason is that in the most general case the mobility is anisotropic, expressed by a tensor $\hat{\mu}$. For example, in an organic crystal, the mobility can be higher in the direction of a particular lattice vector, e.g. due to a smaller intermolecular distance [16]. The diffusion coefficient $\hat{D}$ is directly related to the mobility of the material and thus a tensor, too. However, in case of an amorphous material, the mobility and the diffusion coefficient can be reduced to a scalar. Even if the charge transition from one molecule to another is locally anisotropic, on a larger length scale as given by the device dimensions, these local variations are averages to an effective isotropic mobility μ_{eff}. Thus, the mobility and the diffusion tensor reduces to a scalar. The same argument applies for polycrystalline materials whose grain sizes are small in comparison to the sample structure, so that individual orientations are equally distributed within the semiconductor. Since these criteria apply to the vertical organic triodes, investigated in this work, further discussions are based on one dimension.

The relation between mobility μ and the diffusion coefficient D is caused by the fact that under thermodynamic equilibrium, drift and diffusion must cancel, leading to the Einstein relation [17]:

$$\frac{D}{\mu} = \frac{k_{\mathrm{B}}T}{q}\,. \tag{2.43}$$

However, if an external electric field is applied to a semiconductor structure, a non-equilibrium situation is achieved in which the above equation does not hold true. One can specify a more generalized Einstein relation

$$\frac{D}{\mu} = \frac{n}{q\frac{\partial n}{\partial E_{\mathrm{F}}}} \tag{2.44}$$

which then depends on the filling of the density of states distribution with the change of the Fermi level $\partial n/\partial E_{\mathrm{F}}$ [17]. For a Gaussian DOS filled with a low number of charges, the charge carrier concentration basically increases with the Fermi level exponentially as indicated in Fig. 2.6

[48]. In this case, one can show that the original Einstein relation of Eq. 2.43 is applicable. At larger charger carrier concentrations, an enhancement of the diffusion coefficient by a factor up to 5 occurs given by Eq. 2.44 [49]. Again, the transition between low and high charge carrier concentration is defined by the relative position of the Fermi level to the equilibrium level. If the Fermi level exceeds the equilibrium level, the increase of the charge carrier concentration with the Fermi level position does not follow a strictly exponential law but increases less strongly anymore, resulting in an enhanced contribution of the diffusion current. As a consequence, the diffusion enhancement factor is more pronounced for large energetic disorder because the charge carrier concentration is much lower for a large width of the Gaussian DOS σ at the position of the equilibrium level ($E_\mathrm{F} = E_\infty$). In general, drift and diffusion currents have to be considered for electrons as well as for holes:

$$j = j_\mathrm{e} + j_\mathrm{h}\,. \tag{2.45}$$

and different mobilities (μ_e and μ_h) and as well as different diffusion constants (D_e and D_h) have to be applied.

The current flow in a semiconductor structure can be determined by a set of equations and boundary conditions. To derive the electric potential, the electrostatic Poisson equation

$$\Delta\Phi = -\frac{\rho(x)}{\epsilon\epsilon_0} \tag{2.46}$$

has to be solved for a spatial distribution of charges $\rho(x)$, which can be either free or fixed. Furthermore, the current and charge continuity

$$\frac{\partial\rho(x,t)}{\partial t} = -\frac{\partial j}{\partial x} - q(G_\mathrm{n}(x,t) - R_\mathrm{n}(x,t)) \tag{2.47}$$

must be fulfilled, as given here for electrons. $G_\mathrm{n}(x,t)$ and $R_\mathrm{n}(x,t)$ are the generation and recombination rates, respectively. Generation of free charge carriers can be realized e.g. by impact ionization due to highly energetic charge carriers or by absorption of photons, whose energy is equal or greater than the energy gap of the semiconductor. In contrast to that, recombination processes decrease the number of free charge carriers either by radiative recombination, e.g. due to emission of photons, or by non-radiative recombination, e.g. by recombination via defect states in the energy gap, referred to as Shockley-Read-Hall recombination [3]. Both, generation and recombination, involve the presence of electrons and holes, so that the corresponding rates usually depend on the product of the concentration of electrons and holes np [3]. If recombination and generation processes can be neglected, the current continuity of a static problem reduces to a simple form

$$\frac{\partial j}{\partial x} = 0 \tag{2.48}$$

which can be seen as the differential form of Kirchhoff's current law. This is typically the case for vertical organic triodes, which are unipolar devices, so that generation and recombination do not play a major role.

Together with Eqs. 2.41, 2.42, and 2.46, the system can be fully described and numerically solved, e.g. by drift-diffusion simulations using the Scharfetter-Gummel algorithm [50]. The exact solution then depends on the boundary conditions, such as the electric potential or the electric field at the

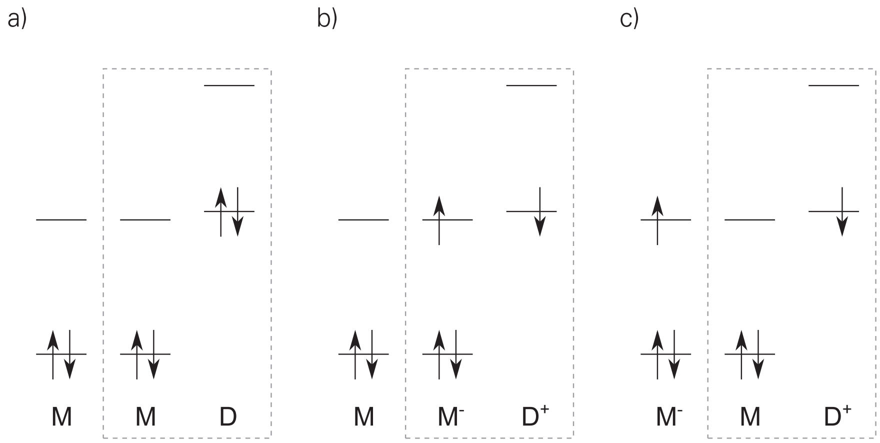

Figure 2.9: Doping in organic semiconductors, explained as a two-step process: a) The matrix molecules *M* and the dopant molecule *D* are neutral. b) Charge transfer from the dopant molecule to a nearest matrix molecule (neighbors surrounded by a gray dashed line). Both molecules are now ionized, but the electron on the matrix molecule is still bound due to the Coulomb interaction between them (charge transfer (CT) complex). c) If the CT complex can be dissociated by the thermal energy, the electron is released to other matrix molecules, where it can freely move.

boundaries of the structure, resulting in a rate of injected charge carriers. Furthermore, the spatial distribution of ionized acceptor or donor states must be included in the charge distribution $\rho(x)$.

Doping of organic semiconductors The controlled variation of spatial conductivity in a semiconductor device by doping is an efficient method to realize high performance devices [51]. To reach such a control, matrix molecules are mixed with a minor concentration of dopant molecules, which are able to release free charge carriers to the matrix. The corresponding increase in layer conductivity of a material is automatically accompanied by a shift of the Fermi energy level toward the transport level. In the case of n-type doping, dopants are used with a HOMO energy level ideally higher or close to the LUMO energy level of the host material, introducing a donor state, as shown in Fig. 2.9. Analogously, the mechanism can be understood for p-type doping, where dopants with low lying LUMO energy values are used, introducing an acceptor state. The smaller the ionization energy and the electron affinity of a molecule are, the more likely it will react with oxygen or water. Thus, n-type dopants are typically more prone to degradation under ambient conditions [52].

Doping can basically be understood as a two-step process:

$$M + \tilde{M}D \rightleftharpoons M + [\tilde{M}^- D^+] \rightleftharpoons M^- + \tilde{M}D^+ \qquad (2.49)$$

where *M* denotes a matrix molecule and *D* a dopant molecule, outlined in Fig. 2.9. First, electron transfer happens from the n-dopant to a neighboring molecule, indicated by $\tilde{M}$. Due to Coulomb interaction, the electron is still bound to the dopant molecule but separated by an intermolecular distance (charge transfer complex $[\tilde{M}^- D^+]$). Upon dissociation, e.g. caused by interaction with lattice vibrations, the electron is released and can now freely move through the organic semiconductor. The dopant molecule itself remains positively ionized. In principle, the second electron of the HOMO level on the dopant molecule might be also released, but this depends on the energetic alignment whether the energy HOMO level after ionization still allows for a further charge transfer. Indicated by Eq. 2.49, the doping process is reversible, and free electrons might be also captured again by dopant molecules. As a result, an effective occupation of the dopant molecule adjusts. The doping efficiency, being the ratio between released charges on average and the number of dopant molecules introduced, is directly affected. Especially, at very high doping concentrations, the occupation of donor states becomes more probable, so that the doping efficiency drops [53]. In contrast, at low doping concentrations, the amount of free charge carriers appears to be reduced in experiment because of charge capturing by trap states. Similarly, this leads to a reduced doping efficiency and a superlinear increase of the conductivity with doping concentration [53, 54]. Nevertheless, a very low doping concentration can be utilized to intentionally fill trap states in order to enhance the charge transport in a molecular layer [31, 54, 55].

2.2.2 Charge injection

Contact formation Free charge carriers in the semiconducting layers of a vertical organic triode can be realized by doping. However, to achieve a continuous current flow through the device, additional charges have to be injected at the contact between a metal electrode and an organic semiconductor. Therefore, the contact formation between both materials, metal and molecules, is of great importance. First, a simplified case will be discussed in which an intrinsic organic semiconductor is placed between two planar metal electrodes. The intrinsic charge carrier concentration of an undoped semiconductor

$$n_\mathrm{i} = N_\mathrm{e} \exp\left(-\frac{E_\mathrm{g}}{2k_\mathrm{B}T}\right) \tag{2.50}$$

is given by the amount of charges which can overcome the energy gap E_g at thermal equilibrium. Organic semiconductor typically have energy gaps larger than 2 eV, so that the intrinsic charge carrier concentration is at maximum in the range of $10^4\,\mathrm{cm}^{-3}$, much lower than the density of states N_e. Nevertheless, even without intentional doping, there will be a certain background charge carrier concentration e.g. due to impurities of the material. This concentration is still low and the semiconductor can be treated as nominally intrinsic. For the moment, interface states are not assumed as they are discussed later.

Figure 2.10 presents the energy alignment of a metal-intrinsic-metal (mim) device. Mim is also referred to as metal-insulator-metal devices which is also applicable to the case here if the charge injection rates from the metal into the organic semiconductor are negligible. In Fig. 2.10a), the materials are presented before a physical contact is made, having independent Fermi energy levels, e.g. characterized by the work function of the cathode $W_\mathrm{f,cat}$ and the anode $W_\mathrm{f,ano}$. Their energy levels are in reference to a common vacuum level E_vac. After joining the materials (s. Fig. 2.10b)), a common Fermi energy level is formed which is constant in the absence of an externally applied voltage $V_\mathrm{a} = 0$. This is achieved by an exchange of charge carriers between the two electrodes of different materials and their work functions. However, the low number of charge carriers in the intrinsic semiconductor leads to a vanishing influence on the energy level alignment. As a consequence, a built-in field originates in the semiconductor because the anode can be assumed to be charged negatively whereas the cathode is charged positively close to the contact. The resulting drop of the electrostatic potential by the built-in potential Φ_{bi} can be seen in the shift of the vacuum energy level.

Energy barriers form between the metal and the organic semiconductor, which an electron has to overcome in order to be injected from either the cathode or anode into the LUMO or HOMO. Principally, one can assume that the rate of injected charge carriers decreases with the height of the energy barrier. This charge injection barrier is predominantly determined by the relative position of the LUMO and HOMO to the Fermi energy level of the metal before making physical contact:

$$\begin{aligned}\Phi_{\mathrm{e}} &= E_{\mathrm{LUMO}} - E_{\mathrm{F}} \\ \Phi_{\mathrm{h}} &= E_{\mathrm{F}} - E_{\mathrm{HOMO}}\end{aligned} \tag{2.51}$$

and they are further related to each other by the energy gap:

$$\Phi_{\mathrm{e,cat}} + \Phi_{\mathrm{h,cat}} = E_{\mathrm{g}} = \Phi_{\mathrm{e,ano}} + \Phi_{\mathrm{h,ano}} . \tag{2.52}$$

The built-in field is not capable to shift them because the potential drop over the infinitesimal small contact region is zero. In order to suppress an effective charge transport in thermal equilibrium, i.e. without external voltage applied, a charge carrier profile will adjusts, leading to diffusion current against the direction of the built-in field, so that the drift and the diffusion current compensate each other.

If an external voltage V_{a} is applied, charge carriers are injected which introduce a non-equilibrium situation. For a positive voltage $V_{\mathrm{a}} > 0$, electrons are injected at the cathode and holes at the anode. Now, a common Fermi level is not able to describe the charge carrier distribution anymore. One solution is to introduce quasi-Fermi levels for electrons ($E_{\mathrm{F,e}}$) and holes ($E_{\mathrm{F,h}}$) which spatially change. This situation is visualized in Fig. 2.10c). One can show that these quasi-Fermi levels define the current flow for each type of charge carriers, separately by

$$j_{\mathrm{e}} = \mu_{\mathrm{e}} n \frac{\partial E_{\mathrm{F,e}}}{\partial x} \quad \text{and} \quad j_{\mathrm{h}} = \mu_{\mathrm{h}} p \frac{\partial E_{\mathrm{F,h}}}{\partial x} \tag{2.53}$$

and thus have to monotonically increase or decrease from one contact to the other [3]. Both currents superimpose and equally contribute to the total current density j. Thus, measuring a current-voltage curve of a sample does not allow for an unambiguous determination of charge injection or charge transport for one type of charge carriers. Only in case of a clear difference in height between the charge injection barriers for electrons and holes, a conclusion can be drawn and related to phenomena associated with one type of charge carrier. For example, assuming that both injection barriers for holes at the cathode as well as at the anode, are considerably large, the current flow realized by holes is negligible and electrons are the dominant charge carriers.

The situation is similar if a negative voltage $V_{\mathrm{a}} < 0$ is applied as shown in Fig. 2.10d). Again, there might be charge injection of both, electrons and holes. However, if the injection barriers for electrons at the cathode and at the anode are highly asymmetric, a current rectifying device (diode), originates. Simultaneously, the hole injection barriers will be similarly asymmetric due to Eq. 2.52. Related to this is a built-in potential $\Phi_{\mathrm{bi}} = eV_{\mathrm{bi}} = \Phi_{\mathrm{e,ano}} - \Phi_{\mathrm{e,cat}}$, which correlates

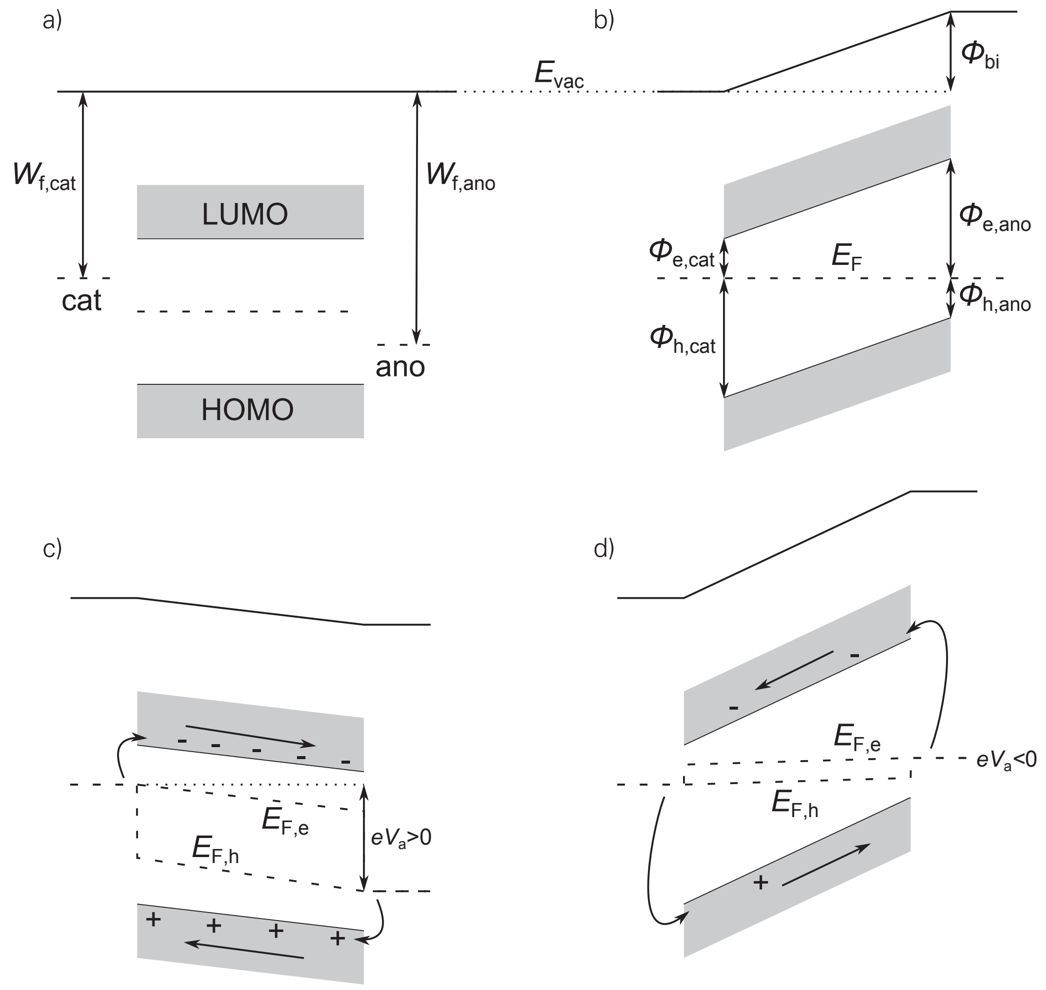

Figure 2.10: Contact formation for an intrinsic semiconductor layer between two metal contacts (cathode (cat) and anode (ano)) with different work function $W_{f,cat}$ and $W_{f,ano}$. a) Materials before contact, having independent Fermi energy levels. b) After the material are in contact, a common Fermi energy level is formed in thermal equilibrium, but the vacuum level E_{vac} changes. Basically, different injection barriers Φ originate for electrons and holes at the cathode as well as at the anode. With applied voltage bias, quasi-Fermi level for electrons ($E_{F,e}$) and holes ($E_{F,h}$) are introduced to characterize the non-equilibrium state.

with the difference in electron injection barriers at the contacts, assuming that the anode has the higher electron injection barrier being thus the rectifying contact. As a consequence, the current through the device will be larger if positive voltages are applied (forward direction) and electrons are injected at the cathode in comparison to similarly high negative voltages (reverse direction). For example, such an asymmetry can be used to rectify signals arising from alternating voltages [56].

The built-in voltage directly influences the current-voltage characteristics, especially in forward direction. At positive voltage smaller than the built-in voltage V_{bi}, there is still an internal electrostatic field, suppressing a contribution of drift current to the total current. Consequently, the current flow through the device is completely determined by diffusion currents [57]. First drift currents through the entire device appear at the flat band condition $V_{\mathrm{a}} = V_{\mathrm{bi}}$. For larger positive voltage, the charge carriers mainly drift through the device although there still might be a substantial contribution from diffusion [58].

Image-force induced barrier lowering As introduced above, the energy values of the charge injection barrier have to be rather understood as ideal values associated with the energy level alignment and the definition of the onset of the conduction and the valence levels. The injection barriers are further altered by the Schottky effect. Each charge carrier injected into a semiconductor interacts with the metal electrodes by introducing an image charge. This image charge behaves like a charge carrier of reverse polarity, having the same distance to the contact as the charge carrier in the semiconductor. The resulting electrostatic potential can then be described by a Coulomb potential:

$$\Phi_{\mathrm{image}}(x) = -\frac{q^2}{16\pi\epsilon\epsilon_0 x} \tag{2.54}$$

where x is the distance from the charge carrier to the interface. This potential is superimposed with a linear potential qFx arising from an externally applied electric field. Figure 2.11 visualizes this situation and it is found that a local potential maximum occurs at

$$x_{\mathrm{m}} = \sqrt{\frac{q}{16\pi\epsilon\epsilon_0|F|}} \tag{2.55}$$

with an energy of

$$\Phi_{\mathrm{B}} = \Phi_{\mathrm{e}} - \Delta\Phi\,, \tag{2.56}$$

effectively lowered by

$$\Delta\Phi = \sqrt{\frac{q|F|}{4\pi\epsilon\epsilon_0}} = 2|F|x_{\mathrm{m}}\,. \tag{2.57}$$

For example, at an electric field of $F = 100\,\mathrm{kV/cm}$, the energy maximum lies at $x_{\mathrm{m}} = 3.0\,\mathrm{nm}$ and the reduction in injection barrier height is around 60 meV ($\epsilon = 4$). Both quantities do not depend on the height of the unaffected energy barrier Φ_{e}, so that the Schottky effect is more relevant for small energies of Φ_{e}, especially at low fields. However, at very large fields the energy barrier between a metal and a semiconductor can be substantially reduced by some 100 meV, which is of the order of the energy barrier height itself. The influence of the image potential on the effective potential quickly decays with the distance of a charge carrier from the metal contact and is negligible after 2 to 3 times x_{m}.

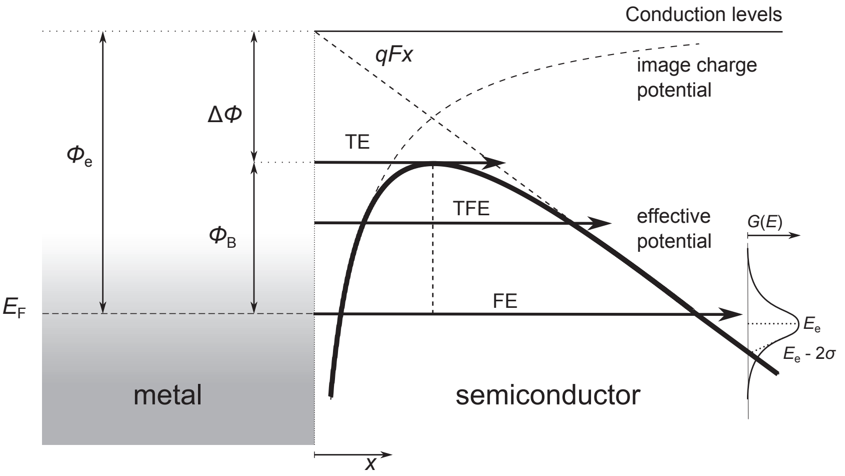

Figure 2.11: Visualization of the Schottky effect (redrawn from Ref. [3, p. 147]). Due to the Coulomb interaction of a charge carrier in the semiconductor with its image charge in the metal, the energy barrier for charge injection is reduced, depending on the strength of the externally applied electric field F.

Charge injection mechanisms The emission of electrons from a metal has been of great interest in the scientific field of vacuum tubes. There, electrons have to overcome an energy barrier of the order of the metal work function to be released to the vacuum. This scenario is similar to the emission of electrons from a metal into a semiconductor, where charges have to overcome the energy barrier Φ_B. A modified version of the equation of this so called thermionic emission (TE) for organic semiconductor is the Richardson-Schottky equation

$$j_{RS} = A^* T^2 \exp\left(-\frac{\Phi_B}{k_B T}\right) \tag{2.58}$$

where

$$A^* = \frac{4\pi e m^* k_B^2}{h^3} \tag{2.59}$$

is the Richardson constant, only depending on the effective mass of the electron m^* in the semiconducting material. The basic relation has been obtained experimentally by Richardson and was later explained by Dushman [59]. It is assumed that electrons high above the Fermi energy level follow Boltzmann statistics, and only electrons with a momentum into the direction of the semiconductor can pass the energy barrier. Figure 2.11 presents the thermionic emission into a potential, considering the Schottky effect. An exact knowledge about the temperature dependence was important at that time because efficient thermionic emission into vacuum was only possible if the metal electrode was heated. For a constant charge injection barrier, the model assumes that independently from the applied voltage, a certain amount of charge carriers can be injected, thus the current saturates with the increase of the electric field. However, due to the Schottky effect, the modulation of the energy barrier causes a continuous increase of j vs. F [3]. In case of organic semiconductors, the theory of thermionic emission can be applied if $\Phi_B \gg k_B T$ and the electric field does not exceed $F = \Phi_B/10\,\text{nm} \sim 1\,\text{MV/cm}$. Above this threshold, one has to assume substantial contributions from tunnel currents through the triangular semiconductor potential, known as field emission (FE). Neglecting the Schottky effect, Fowler and Nordheim found

$$j_{\mathrm{FN}} = \frac{A^*}{\Phi_{\mathrm{B}}} \left(\frac{eF}{\alpha k_{\mathrm{B}}} \right)^2 \exp \left(- \frac{2\alpha \Phi_{\mathrm{B}}^{3/2}}{3eF} \right) \tag{2.60}$$

as the solution of the problem [60]. They argue that the influence of an image potential has a negligible influence onto the effective tunnel current. In contrast to the thermionic emission, the field emission is temperature-independent and hence both processes can be well distinguished.

Electrons with energies between E_{F} and $E_{\mathrm{F}} + \Phi_{\mathrm{B}}$ cannot overcome the energy barrier, but still have the chance to tunnel through the triangular potential barrier (s. Fig. 2.11). This process is called thermionic field emission and the total injected current has to be understood as a sum over all electron energies E [3]. For the extrema, $E = E_{\mathrm{F}}$ and $E = E_{\mathrm{F}} + \Phi_{\mathrm{B}}$, the thermionic field emission coincides with the field emission or the thermionic emission, respectively. With increasing energy of the electrons, the number of electrons participating in an emission process decreases. Simultaneously, the tunnel probability increases if the potential barrier seen by the electron becomes smaller. It then depends on the electric field and the temperature whether TE or FE are dominant.

There are several other factors which have to be considered when describing charge injection into an organic semiconductor, making a prediction difficult. Due to the Schottky effect, the electric potential near the contact leads to drift currents toward the electrode. Thus, the effective current flow over the energy barrier can only be understood by considering diffusion currents [61]. This has led to thermionic-emission-diffusion theory (TED) [3]. Further, charge recombination can occur at the electrode once electrons have been injected [62]. Thus, it is argued that a high charge carrier mobility will positively influence charge injection, according to a larger diffusion length of the charge carriers [3, 61]. Another difference appears for organic semiconductors, showing energetically disordered, localized states. As a consequence, a precise level in the semiconductor defining the charge injection barrier does not exist. The energy barrier Φ_{B} is merely related to the onset of the Gaussian DOS, but the energetic disorder itself influences charge injection. Bässler and coworkers investigated the injection of charge carriers for disordered semiconductors by Monte Carlo simulations, similar to their approach used to describe charge transport [63–65]. They saw that while charge transport might be hindered for large energetic disorder, charge injection becomes even enhanced. One can explain this by considering that some states are shifted closer towards the Fermi energy level of the metal and thus enable efficient charge transfer from the metal to the molecules. I.e., it is more likely to overcome the potential barrier by several small energetic steps than by one large energetic step. The smaller the energetic disorder is, the smaller the injection rates becomes and for negligible energetic disorder or large charge injection barriers Φ_{B}, the solution of the original thermionic emission is obtained [63]. Their simulation did not explicitly include Fowler-Nordheim tunneling, but it was indirectly considered by allowing for hopping events to non-nearest neighbor sites. However, the contributions from these jumps were negligible and the authors state that very high fields (> 1 MV/cm) are necessary before Fowler-Nordheim tunneling becomes relevant for disordered systems. Interestingly, the current-voltage characteristic for injection into a disordered semiconductor can partially resemble those of field emission although the particular process can be excluded. Consequently, deducing the injection mechanism of current-voltage curves has to be done with care and should be supported by e.g. temperature-dependent measurements. In general, one has to assume that charge injection into organic semiconductors is not homogeneously over the contact area. It is more realistic that charge transporting filaments occur according to percolation theory [66]. Nevertheless, thermionic emission and field emission can give a basic understanding how charge carriers are emitted into a semiconducting material from a metal if an energy barrier has to be overcome.

Schottky contact The previous discussion assumes an intrinsic semiconductor. In case of doping, free charge carriers are present in the semiconductor, which interact with the metal and lead to a change in contact formation, see Fig. 2.12 [3]. At first, interface dipoles are not considered ($\Delta = 0$). Assuming that the Fermi energy level of the metal is below the Fermi energy level of the semiconducting material before physical contact exists, electrons are mainly transferred from the semiconductor to the metal until a common Fermi level is established exists after contact. This charge transfer results in a depletion zone of length

$$w_\mathrm{D} = \sqrt{\frac{2\epsilon\epsilon_0}{qN_\mathrm{d}}\left(V_\mathrm{bi} - V_\mathrm{a} - \frac{k_\mathrm{B}T}{q}\right)} \tag{2.61}$$

close to the contact, which varies by changing the applied voltage V_a [3]. Here, N_d is the concentration of free charge carriers realized by n-type doping. Because positive donor states remain there, this region is also called a space charge zone. The amount of positive charges in the semiconductor and negative images charges in the metal is equal, causing an electric field, dropping over the depleted zone, according to Fig. 2.12. As a consequence, a built-in potential Φ_bi originates. The corresponding built-in voltage V_bi depends on the height of the charge injection barrier referred to as the Schottky-barrier Φ_B and on the difference in energy between the LUMO and the Fermi energy level of the doped but neutral semiconductor. Thus, one can assume that the built-in voltage increases for increasing doping concentration.

Equation 2.61 is of great technological importance since the depletion zone can be related to a depletion capacitance per unit area by

$$C_\mathrm{D} = \frac{\epsilon\epsilon_0}{w_\mathrm{D}}\,. \tag{2.62}$$

Thus, from measuring the capacitance, one can obtain valuable information about the doping concentration

$$N_\mathrm{d} = \frac{2}{q\epsilon\epsilon_0}\left(-\frac{1}{dC^{-2}/dV}\right) \tag{2.63}$$

from the corresponding Mott-Schottky relation [3]. Since the depletion length does not depend on the charge carrier mobility of the material, Eq. 2.63 enables a convenient characterization of doping in semiconductors [32]. However, the derivation bases on the assumption that the space charge in the depletion zone is homogeneously distributed, which applies only for strong depletion, so that the depletion length should be large in comparison to the decay profile of the charge carrier concentration, characterized by the Debye length

$$L_\mathrm{D} = \sqrt{\frac{\epsilon_\mathrm{s}\epsilon_0 k_\mathrm{B}T}{q^2 N_\mathrm{d}}}\,. \tag{2.64}$$

This length gives a lower limit to resolve abrupt changes of N_d within the electric potential Φ. For example, at a doping density of $10^{16}\,\mathrm{cm}^{-3}$, the Debye length is about 40 nm whereas at

$10^{19}\,\mathrm{cm}^{-3}$, values close to 1 nm can be estimated [3], depending further on the permittivity ϵ_s of the semiconductor [3].

The Schottky-barrier itself does not depend on the doping concentration and remains constant, but it is indirectly influenced by the Schottky effect, modulating the height by the electric field arising in the depletion zone. Hence, the image-force induced barrier lowering becomes the stronger the larger the doping concentration is. As a consequence, the contact resistance decreases. Moreover, large doping concentrations result in a small depletion length, so that field emission becomes the dominating injection mechanism [3]. Thus, heavily doped semiconductors lead to Ohmic contacts which have a negligible resistance in comparison to the resistance arising from charge transport in the semiconductor layer.

Modifications of the above theory arise from interface dipoles which introduce an abrupt change in energy at the contact [67]. Therefore, the energy level of the vacuum is shifted by an energy Δ. Related to this, the Schottky-barrier and the built-in voltage changes by the same amount, affecting the depletion length. Mathematically, such interface dipoles are described as infinitesimally thin, corresponding to the length δx in Fig. 2.12. In reality, they extend over a few Å. Interface dipoles are related to a charge displacement at the contact, as listed by Ishii *et al.* [68]. They can e.g. arise from interface states between the metal and the semiconductor, as indicated in Fig. 2.12, where charges are trapped in accordance with the Fermi-Dirac statistics. As a consequence, the potential drop at the contact area changes. Other origins might be dopant molecules in contact to the metal, forming an anion or cation by charge transfer between the molecule and the metal. For example, this effect is used for contact doping, where a thin layer of pure dopants realizes an Ohmic contact between a metal and an undoped semiconductor [69, 70]. Interface dipoles can also be introduced by polar molecules whose internal electric field leads to a potential shift at the contact or by a chemical reaction between molecules and the metal surface, to name a few [71, 72]. As a consequence, the formation of the contact can hardly be predicted and has to be studied experimentally, e.g. by photoelectron spectroscopy, for each material system individually.

Furthermore, a detailed understanding of processes taking place at the contact is hampered by the morphology of the interface. Above, it was assumed that the metal is absolutely flat and the molecules have an equal orientation to the metal. These are strong idealizations. Thin metal films are typically not fully flat and are polycrystalline, so that locally the work function might vary [68]. Likewise, the organic semiconductor can have a polycrystalline phase and the molecular orbitals are differently aligned towards the metal surfaces. If a metal film is deposited on a molecular layer, metal atoms are likely to diffuse into the organic semiconductor layer, which makes an adequate description highly complex [73]. Thus, the contact formation highly depends on the fabrication procedure and their parameters [49]. A larger overview concerning this topic can be found elsewhere [74].

2.2.3 Limitations of the current

The current flow through a semiconducting layer can be either limited by the amount of charges injected at the contact, associated with injection limited currents (ILC), or by charge crowding in

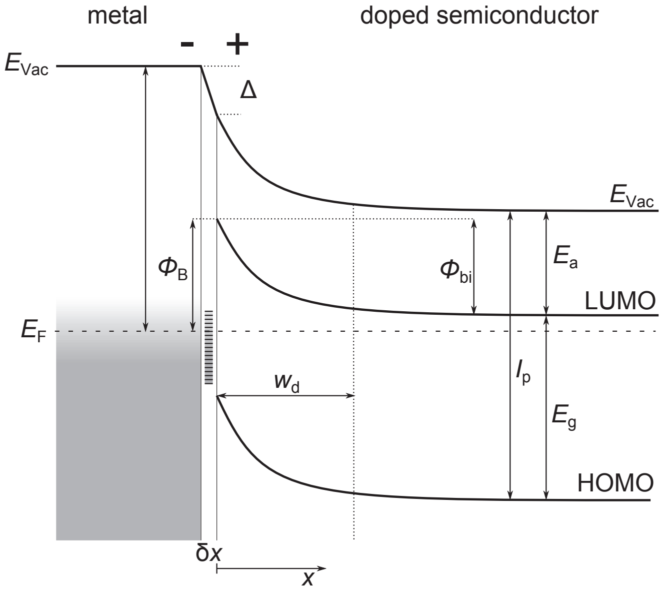

Figure 2.12: Formation of a Schottky contact between a metal and a doped semiconductor. Charge transfer from the semiconductor to the metal causes a potential drop over a depleted region w_{D}, so that the Fermi energy level of both materials align under thermal equilibrium. An interface dipole of energy Δ introduces an abrupt shift in the energy level alignment at the contact.

the layer, associated with space charge limited currents (SCLC). For both cases, Fig. 2.13 presents the distribution of the charge carrier concentration n, the electric potential Φ, and the electric field F for a semiconductor structure of length L, sandwiched between two metals with a difference in electric potential due to the applied voltage V_{a}. The charge flow of electrons is assumed to be from the left to the right in accordance with the gradient of the electric potential. All charge carriers are generated due to injection and the charge carrier mobility is assumed to be constant. A contribution from diffusion current is not considered [75].

If the injection barrier for electrons is large, the current flow through the semiconductor is limited by the amount of charges injected per time and area [16]. Then, the corresponding injection rate r_{inj} determines the current density

$$j = er_{\mathrm{inj}}(F) \tag{2.65}$$

which depends on the electric field

$$F(x) = \frac{V_{\mathrm{a}}}{L} = \text{const.} \tag{2.66}$$

which is constant all across the whole layer, thus applying also at the injection contact. The electric potential

$$\Phi(x) = -V_{\mathrm{a}}\frac{x}{L} \tag{2.67}$$

drops linearly from 0 to $-V_{\mathrm{a}}$. The reason is that the charge carrier concentration in the device resulting from the injected charge carriers is too low to realize a relevant interaction. As a consequence, the charge carriers are homogeneously distributed within the device, given by

$$n(x) = \frac{jL}{e\mu V_\mathrm{a}} = \text{const.} \tag{2.68}$$

The situation changes if the injection barrier is small. Often, this is associated with an Ohmic contact, which does not mean that the dependence of the injection rate on the electric field is linear, but rather that the bulk characteristic of a semiconductor structure with a linear current-voltage relation would be measurable. Now, the current density is given by the charge carrier mobility of the material and the charge carrier concentration which is in accordance with the Poisson equation and the current continuity [16]. One can show that now charges piles up at the injecting contact where they form a space charge region, described by

$$n_\mathrm{SCLC}(x) = \frac{3\epsilon\epsilon_0}{4eL^2}\sqrt{\frac{L}{x}}V_\mathrm{a}\,. \tag{2.69}$$

This effect can be interpreted as the result of a semiconductor structure which is not able to conduct all injected charges away under the assumption of a constant electric field. Then, the locally higher charge carrier concentration raises the electric potential

$$\Phi_\mathrm{SCLC}(x) = -\left(\frac{x}{L}\right)^{3/2} V_\mathrm{a} \tag{2.70}$$

close to the contact and reduces the electric field

$$F_\mathrm{SCLC}(x) = \frac{3}{2L}\sqrt{\frac{x}{L}}V_\mathrm{a} \tag{2.71}$$

at the injecting contact, so that the injection rate of charge carriers is lowered. In contrast, the electric field near the ejecting contact is even enhanced in comparison to a linear potential drop for the same applied voltage V_a. Thus, charges are more effectively conducted in this range.

It is seen from Eqs. 2.69-2.71 that the profiles of the charge carrier concentration, the electric potential, and the electric field changes linearly with the applied voltage, but qualitatively remain unchanged. I.e., to increase the current through the device, the charge carrier concentration increases everywhere by the same factor. However, the current density given by the Mott-Gurney equation

$$j_\mathrm{SCLC} = \frac{9}{8}\epsilon\epsilon_0\mu\frac{V_\mathrm{a}^2}{L^3} \tag{2.72}$$

does not scale linearly with applied voltage, but rather shows a quadratic dependence as a characteristic feature of space charge limited currents [76]. One can explain this by the fact that both, the charge carrier concentration as well as the electric field, contribute with their linear dependencies on the applied voltage. Further, the current density scales linearly with the charge carrier mobility. Since the charge carrier concentration already depends on the applied voltage it does not explicitly enter into Eq. 2.72. As a consequence, the regime of SCLC, identified by its voltage dependence, can be used to estimate the charge carrier mobility of semiconducting materials. Note that there might also be other effects leading to a square dependence on the applied voltage. To distinguish ICL and SCLC, one can compare devices of different length at the same mean electric field V_a/L. Then, Eqs. 2.72 and 2.65 reveal that currents through thicker devices are more

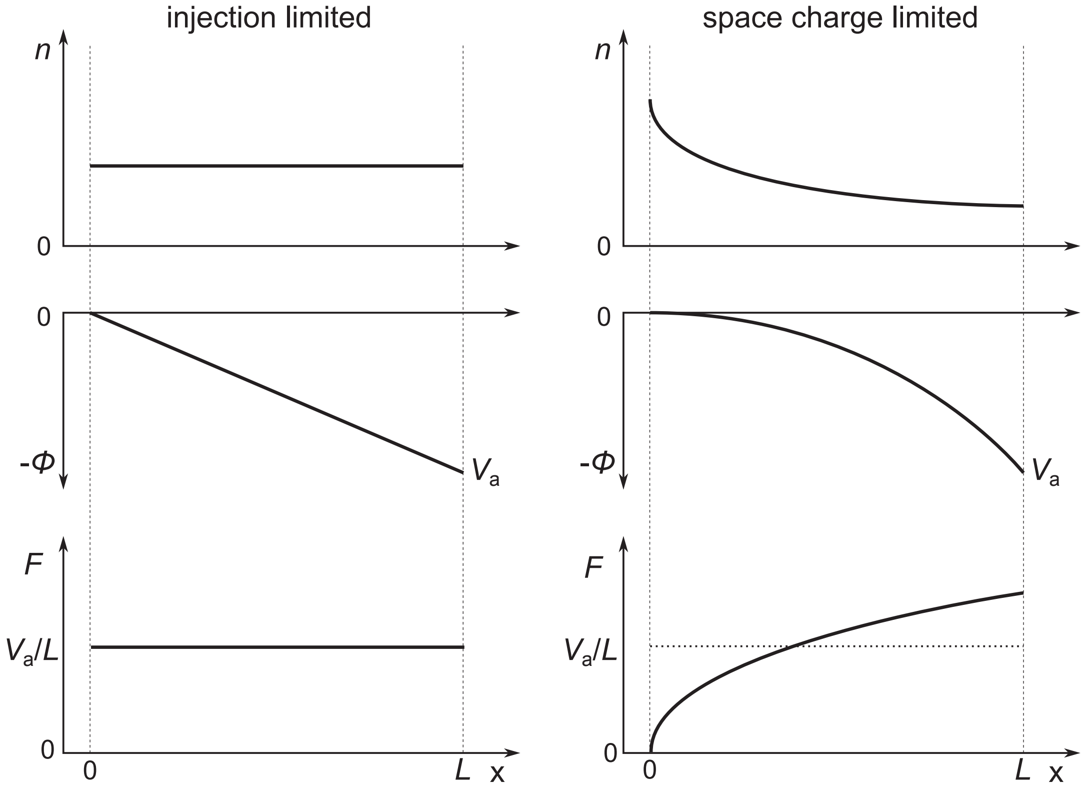

Figure 2.13: Comparison of injection limited currents and space charge limited currents. Shown are the distribution of charge carrier concentration *n*, the electric potential Φ along the direction of the electric field *F* in the material.

hampered by space charges whereas the current in devices with an injection limitation remain unchanged.

The theory described above has been presented for an ideal semiconductor showing either negligible contact resistance or large contact resistance. In reality, the contact resistance decreases with the electric field by an exponential function which is much stronger than the reduction of layer resistance predicted by space charge limited currents. Then, both regimes can be present in the same device. At low voltage, an injection limitation is present, whereas at higher voltage, a transition to a space charge limitation occurs. Further deviations might arise from a non-constant mobility as observed for organic semiconductors. For rising voltages, charge carrier concentration and electric field increase, both influencing on the charge carrier mobility. The typical square dependence on the applied voltage does not hold true anymore, and assuming that the mobility increases with the applied voltage, a $j \propto V^{\alpha}$ law with $\alpha > 2$ can be expected. SCLC theory does also not consider diffusion of charge carriers [75]. For injection limited devices, diffusion plays a minor role because the charge carrier concentration is constant. However, devices with small dimensions and high charge carrier concentrations might show substantial contributions from diffusion currents. For example, de Bruyn *et al.* studied metal-insulator-metal diodes and found a non-neglectable influence of diffusion currents even beyond the built-in voltage [57]. In general, the built-in voltage has to be considered when evaluating SCLC, reducing the applied voltage, effectively. Another influence onto SCLC arises from trap states [77]. As long as they are not permanently filled, so that charges can interact with them, the mobility μ of the semiconductor seems to be reduced to an effective mobility μ_{eff}. Nevertheless, Eq. 2.72 still applies [16]. Only after all traps are filled, the mobility raises to its original value obtained for a trap-free semiconductor structure.

The previous considerations assume that all charge carriers in the semiconducting layer are injected at the contact. However, due to intentional doping or impurities, a constant charge carrier concentration might already be established if a voltage is not applied. The voltage from which on SCLC can be obtained is related to the point where the charge carrier concentration realized by charge injection, see Eq. 2.69, exceeds the one already present in the layer. Otherwise, at moderate electric fields where the charge carrier mobility is hardly influenced, purely Ohmic behavior of the current-voltage characteristic can be obtained. This is visualized in Fig. 2.14 for a background charge carrier concentration $n_0 = 2 \times 10^{15}\,\text{cm}^{-3}$, a device length $L = 100\,\text{nm}$, a relative permittivity $\epsilon = 4$, and a constant mobility of $\mu = 0.01\,\text{cm}^2/\text{Vs}$. At low voltages, the conductivity is determined by charges already present in the layer, resulting in a linear current-voltage curve. Above the transition voltage $V_{\text{tr}} = 0.08\,\text{V}$ on, a SCLC arises with the typical $j \propto V^2$ dependence. The background charge carrier concentration

$$n_0 = \frac{9\epsilon\epsilon_0}{8eL^2} V_{\text{tr}} \tag{2.73}$$

can be determined from the transition point by comparing Eq. 2.72 with Eq. 2.41. Interestingly, this equation does not depend on mobility, allowing for a simple estimation of the charge carrier concentration in homogeneously doped layers [78].

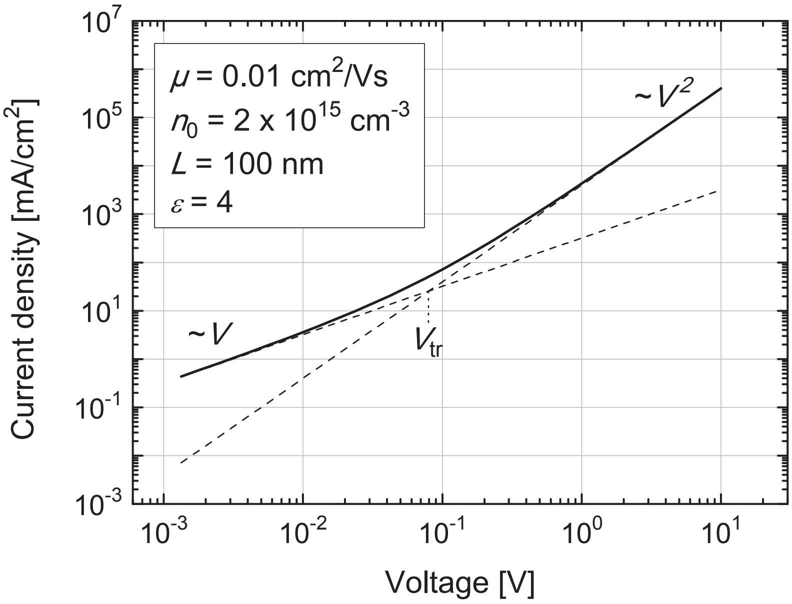

Figure 2.14: Space charge limited current in the presence of a background charge carrier concentration n_0. At low voltages, one finds a linear current-voltage dependence which changes to quadratic after the transition voltage V_{tr}.

2.2.4 Metal-oxide-semiconductor structures

A Schottky diode is basic device using a combination of a slightly doped layer and highly doped layer in order to achieve a Schottky contact (rectifying) and an Ohmic contact with their adjacent metal electrodes. A non-symmetric current-voltage characteristic results, following the diode equation

$$j = j_0 \left[\exp\left(-\frac{qV_a}{\eta k_B T} \right) - 1 \right] \tag{2.74}$$

where j_0 is the current injected at the Schottky contact which generally depends on voltage due to image-force induced barrier lowering. The factor η is the ideality factor, typically close to 1 in case of inorganic semiconductors, but somewhat larger for organic semiconductors (2-4) [3, 79].

New physics is obtained if an insulator, typically an oxide of thickness t_{ins}, is embedded at the interface of the Schottky contact, realizing a metal-oxide-semiconductor (MOS) structure. As the insulation prevents any current flow, capacitive characteristics of this device dominates, so that it is referred to as a MOS capacitor. Figure 2.15 visualizes the energy level alignment of an n-tpye MOS capacitor for the three cases: negative bias, without bias, and positive bias. At thermal equilibrium, a space charge zone develops in the semiconductor close to the insulator as the consequence of the Fermi level alignment between metal and semiconductor. Depending on the relative Fermi level positions of the materials before contact, this zone might be charged positively or negatively. Here, it is assumed that the Fermi level of the semiconductor is closer to the vacuum energy level at the beginning, so that depletion occurs, according to Eq. 2.61, and introduces a built-in voltage. This also leads to a potential drop over the insulator. The electric field in the insulator and in the depletion zone can be assumed to be similar, only differing by the ratio of the permittivities ϵ_{ox} and ϵ_s of both materials. Nevertheless, an effective current flow is

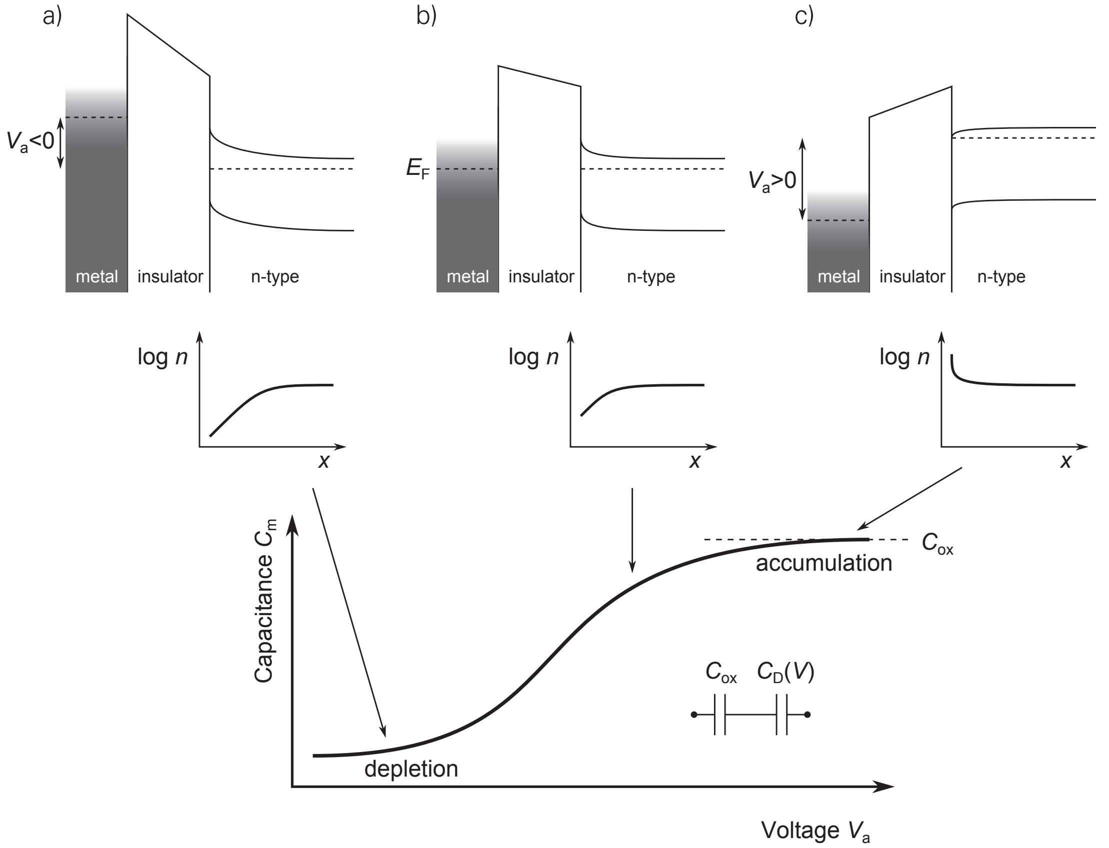

Figure 2.15: Energy alignment of an n-type MOS capacitor a) at negative bias, b) without bias c) at positive bias. The structure consists of a metal, an insulator, and an n-type semiconductor. At negative voltages, the semiconductor is increasingly depleted, leading to the depletion capacitance C_D. At positive voltages, charges accumulate in front of the insulator, enabling the measurement of the oxide capacitance C_{ox} in a capacitance-voltage measurement.

not present in the device, indicated by the flat Fermi level. In all cases, the drift and diffusion currents compensate each other.

For negative voltages, the depletion zone grows and the related capacitance per unit area C_D shrinks. In this case, the applied voltage V_a drops over the oxide and the depletion zone. Generally, the measured capacitance

$$C_\mathrm{m} = \frac{C_\mathrm{ox} \cdot C_\mathrm{D}}{C_\mathrm{ox} + C_\mathrm{D}} \tag{2.75}$$

has to be understood as a series connection of the oxide capacitance $C_\mathrm{ox} = \epsilon_\mathrm{ox}\epsilon_0/t_\mathrm{ins}$ and the depletion capacitance C_D. However, for $C_\mathrm{D} \ll C_\mathrm{ox}$, the depleted semiconductor dominates the capacitive behavior of the device, and by using Eq 2.63, the doping concentration of the semiconductor can be studied by the voltage dependence of C_D. For large negative voltages, the Fermi level even shifts away from the conduction levels towards the valence levels of the semiconductor. According to that, after a deep depletion, a charge carrier inversion occurs (not shown in Fig. 2.15) near the interfacial region at the insulator [3]. Then, holes accumulate there, although the semiconductor is n-type doped. For low bandgap materials like inorganic semiconductors, this inversion can be realized by intrinsically generated charge carriers, a rather slow process, so that the capacitance-voltage dependence reveals this behavior only at low frequencies [3]. For large bandgap materials, like organic semiconductors, the inversion due to intrinsically generated charge carriers has not been seen because the corresponding frequency regime would be shifted to extremely low values. However, inversion in organic semiconductors has been recently demonstrated by the help of externally injected charge carriers [80].

In vertical organic triodes, the focus lies on accumulation and depletion of majority charge carriers (i.e. electrons) because inversion does not play a role as outlined in the results (cf. Sec.7). Accumulation of electrons basically occurs for applying positive voltages. Then, the electric field at the insulator is reversed to the case of depletion. The charge carrier density in the narrow accumulation zone is large and reaches values close to a tenth of the density of states. For that reason, the electric field is screened by the charge accumulation and nearly the entire applied potential drops over the insulator. The charge carrier profile reveals a sharp decrease of the charge carrier concentration with the distance from the insulator-semiconductor interface and after a few nanometers, the original doping concentration is reached. Accordingly, the amount of accumulated charge carriers can be denoted by $Q = C_\mathrm{ox} V_\mathrm{a}$. Since the depletion is not present anymore, the corresponding capacitance of the organic materials vanishes and the measurable capacitance is equal to the oxide capacitance $C_\mathrm{m} \sim C_\mathrm{ox}$, as visualized in Fig. 2.15.

Deviations from this behavior occur for MOS capacitors with insulating layers with a thickness of a few nanometers, called MOS diodes [81, 82]. They exhibit substantial leakage current through the oxide due to quantum-mechanical tunneling [83–85]. It is caused by the fact that the wave function of an electron even extends into regions where the local potential $\Phi(x)$ is higher than its energy E. For finite potential barriers, electrons have a certain probability to be transmitted through the potential due to their probability of presence behind the barrier. This requires that both states contributing to the tunneling process are of equal energy. In general, the tunnel current through an arbitrary potential is given by

$$j_\mathrm{t} = \frac{4\pi q m^*}{h^3} \int_0^{E_\mathrm{F}} dE \int_0^{E} T(E, E_\perp) dE_\perp \,, \tag{2.76}$$

where $E_\perp$ is the transverse energy of the electrons related to the transverse momentum, E is the total kinetic energy of the electrons, and the transmission probability

$$T(E) = \exp\left(-\frac{2}{\hbar}\int_0^{t_\text{ins}} \sqrt{2m^* E_\perp - 2m^*_\text{ox}(E - \Phi(x))}dx\right) \tag{2.77}$$

decreases with the height of the potential $\Phi(x)$ and the thickness of the oxide t_ins [85]. For arbitrary potential profiles, one can numerically solve these equations by using a transfer matrix approach [86]. The presence of direct tunneling (DT) is characteristic for very thin oxides ($t_\text{ins} < 3\,\text{nm}$) [3, 83, 85, 87]. In this case, the voltage drop over the oxide is smaller than the energy barrier height between the Fermi energy level and the conduction band of the oxide, leading to a trapezoidal shaped potential. If larger voltages are applied, the potential becomes triangular and electrons can tunnel into the conduction band of the oxide instead of tunneling through the entire oxide layer according to Fowler-Nordheim tunneling. For larger thickness of the oxide, Fowler-Nordheim tunneling will automatically be the dominant process. Likewise to the contact formation, the Schottky effect has to be considered, which can substantially lower the energy barrier introduced by the oxide, leading to deviations from a simple triangular shape of the potential profile [88]. Thus, deriving analytical solutions is relatively complicated and the reader is referred to the references [3, 85, 87–89] for explicit expressions. In general, the tunnel current only weakly depends on temperature, which clearly distinguishes tunneling from other charge transport mechanisms.

The characteristic of a MOS diode can be seen as a mixture of a Schottky diode with current rectifying behavior and a MOS capacitor because of the device capacitance which shows features of depletion or accumulation [90]. In comparison to Schottky diodes, the highest currents in forward direction might be reduced due to the presence of the oxide, and the ideality factor typically increases the thicker the insulating layer is [3]. The high leakage current also introduces deviations from an ideal capacitance-voltage characteristic as obtained for MOS capacitors. In order to obtain the correct oxide capacitance, one has to ensure that the series resistances within the device do not limit charging of the oxide capacitance, which is typically larger than $1\,\mu\text{F/cm}^2$ [90, 91]. Otherwise, measured capacitances at positive voltage are underestimated. Besides that, the high conductance of the oxide layer leads to reduced values at positive voltages, as well [92].

MOS structures are applied in field-effect transistors (FET), because they allow for the control of the conductivity in the accumulation or inversion zone by orders of magnitude. Nowadays, the device dimensions are aggressively downscaled to maximize the integration density [84]. Accordingly, the operation voltages can be decreased, reducing the power consumption, but the oxide capacitance has to increase in order to achieve a similar conductivity of the charge accumulation zone. For that reason, the oxides of modern MOSFETs in processors for consumer electronics, like personal computers or mobile phones, are extremely thin [83]. The thickness of the standard silicon dioxide layer used as the dielectric in MOSFETs has been 1.4 nm for many years [93]. Hence, MOS structures employed in transistors have to be understood as MOS diodes and thus are of great relevance. The leakage current through the oxide can be accepted up to a certain level, especially if the transistor operates at highest switching speed (cf. Sec. 3.3.5). New design strategies try to find materials with a large permittivity, so that the oxide thickness can be increased without reducing the oxide capacitance necessary to accumulate large charge concentrations at low voltages [93]. It will be shown by this work that MOS diodes are also the basic component of a vertical organic triode.

2.3 SELF-HEATING THEORY OF THERMISTOR DEVICE

Self-heating phenomena were first studied in the investigation of the electrical breakdown of dielectrics induced by a thermal runaway [94, 95], where above a certain threshold voltage, the cooling of the device is no more sufficient to keep the system in a stationary state. Furthermore, self-heating induces many thermal runaway and switching phenomena, e.g. in chemical reactions [96], thermistors [97, 98], semiconductors [99, 100], and transport through thin films [101–103]. For solid state electronic devices, it is well known that due to electrothermal feedback, regions of negative differential resistance (NDR) can appear in the current-voltage characteristic, see Fig. 2.16 [104].

For materials with an Arrhenius-like conductivity vs. temperature dependency, NDR phenomena such as thermal switching induced by self-heating only occur for activation energies $E_{\mathrm{act}} > 4\,k_{\mathrm{B}}T_{\mathrm{a}}$, where k_{B} denotes Boltzmann's constant and T_{a} the ambient temperature [104]. The motivation to expect NDR in organic semiconductors is given by the basic organic mobility model for low fields and low densities described by

$$\mu(T) = \mu_0 \exp\Big[-C\Big(\frac{\sigma}{k_{\mathrm{B}}T}\Big)^2\Big],$$

where σ is describing the disorder of energy levels, and $C \approx 0.4$ [21, 105]. The mobility is increasing with the temperature and can be locally approximated by an Arrhenius law with an activation energy $E_{\mathrm{act}} = 2C\sigma^2/(k_{\mathrm{B}}T_{\mathrm{a}})$. Typical values of the disorder parameter $\sigma = (2-6)\,k_{\mathrm{B}}T_{\mathrm{a}}$ result in activation energies between about $3\,k_{\mathrm{B}}\,T_{\mathrm{a}}$ and $30\,k_{\mathrm{B}}T_{\mathrm{a}}$. However, the activation energy may be reduced due to a dependence on the carrier density, see [105] for a detailed discussion. Finally, injection as well as energy barriers between adjacent organic layers in the range of several tenth of an eV should be mentioned as a reason for temperature activated charge transport [106].

Since activation energies above $4\,k_{\mathrm{B}}T_{\mathrm{a}}$ are quite common in organic semiconductors, electrothermal bistability or NDR phenomena due to the positive feedback between Joule heating and conductivity have to be expected. Indeed, it has been mentioned in literature that thermal runaway might be the reason for device breakdown [107, 108].

Theory of positive temperature feedback In the following, it is assumed that the isothermal current-voltage relation for the circuit is given by a power law

$$I_{iso}(V,T) = I_{\mathrm{ref}}\left(\frac{V}{V_{\mathrm{ref}}}\right)^{\alpha} F(T) \tag{2.78}$$

with a positive exponent α and a temperature-dependent conductivity factor $F(T)$ resulting from an Arrhenius law

$$F(T) = \exp\left[-\frac{E_{\mathrm{act}}}{k_{\mathrm{B}}}\left(\frac{1}{T}-\frac{1}{T_{\mathrm{a}}}\right)\right]. \tag{2.79}$$

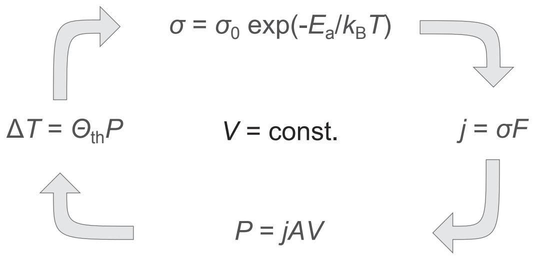

Figure 2.16: Positive feedback loop for self-heating. For a constant voltage V, a current flow j results in a power dissipation P which in turn causes a temperature rise ΔT. As a consequence, the temperature activated conductivity σ increases and thereby again the current flow.

The quantities V_{ref}, I_{ref}, and $P_{\mathrm{ref}} = V_{\mathrm{ref}} I_{\mathrm{ref}}$ denote reference values for voltage, current, and power, respectively. The homogeneous steady states of the device are given by equilibria of the global heat balance equation, expressing that the dissipated Joule power $\dot{Q}_2 = IV$ equals the heat loss $\dot{Q}_1 = \frac{1}{\Theta_{\mathrm{th}}}(T - T_{\mathrm{a}})$ to the surrounding described by the thermal resistance Θ_{th},

$$\frac{1}{\Theta_{\mathrm{th}}}(T - T_{\mathrm{a}}) = P_{\mathrm{ref}} \left(\frac{V}{V_{\mathrm{ref}}}\right)^{\alpha+1} F(T). \tag{2.80}$$

For temperatures $T \geq T_{\mathrm{a}}$, the self-consistent current-voltage characteristic including self-heating can be parametrized by combining Eqs. (2.78) and (2.80),

$$V(T) = V_{\mathrm{ref}} \left(\frac{T - T_{\mathrm{a}}}{\Theta_{\mathrm{th}} P_{\mathrm{ref}}}\right)^{\frac{1}{\alpha+1}} F(T)^{-\frac{1}{\alpha+1}}, \tag{2.81}$$

$$I(T) = I_{\mathrm{ref}} \left(\frac{T - T_{\mathrm{a}}}{\Theta_{\mathrm{th}} P_{\mathrm{ref}}}\right)^{\frac{\alpha}{\alpha+1}} F(T)^{\frac{1}{\alpha+1}}. \tag{2.82}$$

Different points on the self-consistent current-voltage characteristic correspond to different values of the temperature rise $T - T_{\mathrm{a}}$. The differential resistance of the corresponding IV curve has the form

$$\frac{dV}{dI} = \frac{1 - (T - T_{\mathrm{a}})\frac{d}{dT}\ln F(T)}{\alpha + (T - T_{\mathrm{a}})\frac{d}{dT}\ln F(T)} \frac{V}{I}. \tag{2.83}$$

For $T - (\frac{d}{dT}\ln F(T))^{-1} > T_{\mathrm{a}}$, a region of negative differential resistance is obtained. In the Arrhenius type temperature dependence Eq. (2.79), a NDR region only appears for activation energies $E_{\mathrm{act}} > 4\,k_{\mathrm{B}} T_{\mathrm{a}}$. This can be seen in Fig. 2.17, where the self-consistent IV curve of such an intrinsic device according to Eqs. (2.81) and (2.82) is shown for an isothermal Ohmic current-voltage relation ($\alpha = 1$, $V_{\mathrm{ref}}/I_{\mathrm{ref}} = 2000\,\Omega$).

The turnover points of the S-shaped IV curve are characterized by the condition $\frac{dV}{dI} = 0$. For $E_{\mathrm{act}} > 4\,k_{\mathrm{B}} T_{\mathrm{a}}$, irrespective of the exponent α in Eq. (2.78), the temperature increase at the two turnover points $\Delta T_{1,2} = T_{1,2} - T_{\mathrm{a}}$ becomes

$$\frac{\Delta T_{1,2}}{T_{\mathrm{a}}} = \frac{E_{\mathrm{act}}}{2 k_{\mathrm{B}} T_{\mathrm{a}}} \left(1 \mp \sqrt{1 - \frac{4 k_{\mathrm{B}} T_{\mathrm{a}}}{E_{\mathrm{act}}}}\right) - 1. \tag{2.84}$$

The temperature rises at the turnover points depend only on the normalized activation energy, $E_{\mathrm{act}}/(k_B T_a)$. Along the S-shaped current-voltage characteristics, two stable branches exist: an 'ON' state with high conductivity and an 'OFF' state with low conductivity, whereas the intermediate NDR region is unstable for constant voltages, see Fig. 2.17. This bistable behavior of the IV characteristic is related to thermal switching at the turnover points with $dI/dV \to \infty$, involving a hysteresis loop [109, Ch. 6.2], where the switching between the low conductivity OFF and the high conductivity ON branches occurs.

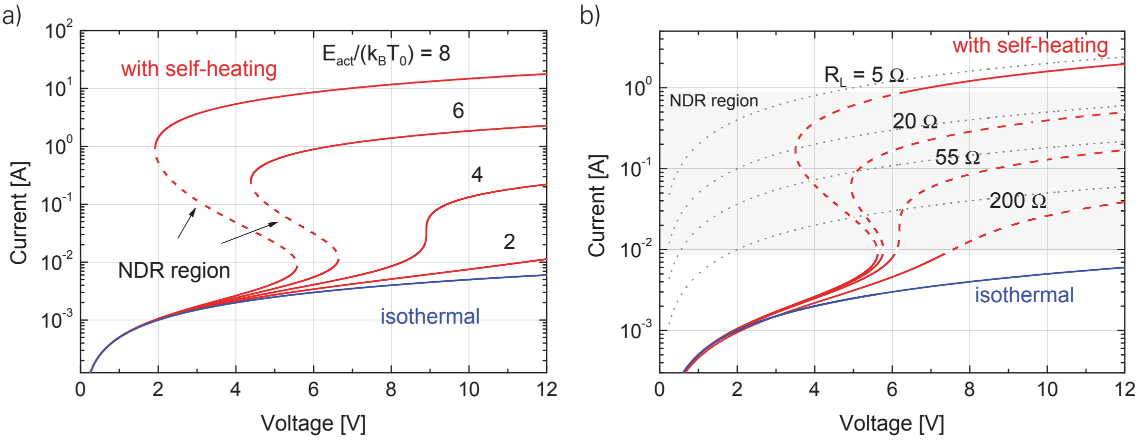

Figure 2.17: a) Self-consistent current-voltage characteristics including self-heating according to Eqs. (2.81) and (2.82) (red), revealing that thermal switching can only occur above the critical value of the activation energy, $E_{\mathrm{act}} > 4\,k_B T_a$. Unstable NDR regions are indicated by dashed lines. Thermal resistance $\Theta_{\mathrm{th}} = 1000\,\mathrm{K/W}$. Blue: isothermal current-voltage relation (2.78) with $\alpha = 1$ at ambient temperature $T_a = T_0 = 293\,\mathrm{K}$. b) Calculated current-voltage characteristics of an electrical circuit consisting of a device including self-heating, together with a load resistance R_L in series (red), for $E_{\mathrm{act}} = 8\,k_B T_a$, a thermal resistance $\Theta_{\mathrm{th}} = 1000\,\mathrm{K/W}$, and different values of the load. The dashed parts indicate the NDR region of the intrinsic device as shown in Fig. 2.17. Blue: isothermal current-voltage relation (2.78) with $\alpha = 1$ at constant temperature T_a, black dotted: load resistance only.

The IV characteristics of the intrinsic device showing the pure S-shaped NDR (S-NDR) behavior described by Eqs. (2.81) and (2.82) together with a load resistance R_L in series can again be parameterized by an increased temperature $T \geq T_a$. The resulting characteristic $(V_{\mathrm{tot}}(T), I(T))$ involves a modified total voltage along the load line $V_{\mathrm{tot}}(T) = V(T) + R_L I(T)$, where $V(T)$ and $I(T)$ are defined in Eqs. (2.81) and (2.82), respectively. Turnover points are characterized by $\frac{dV}{dI} + R_L = 0$, corresponding to a tangency condition for the intersection points between the load line and the IV characteristic of the S-NDR element itself [99, 109, Ch. 6.2]. For sufficiently small load resistance, namely for $-\min\left(\frac{dV}{dI}\right) > R_L$, the hysteresis effect is preserved, so that thermal switching between the ON and OFF states remains possible. The impact of a load resistance on the IV characteristic of the circuit calculated for a device with linear isothermal IV relation ($\alpha = 1$, $V_{\mathrm{ref}}/I_{\mathrm{ref}} = 2000\,\Omega$) is shown in Fig. 2.17. By an appropriate choice of the load resistance, it may be possible to reduce the dissipated power in the ON state to a value that does not destroy the device by thermal runaway, but still preserves thermal switching. A further increase of the load resistance suppresses thermal switching ($R_L > 55\,\Omega$ in Fig. 2.17), leading to a stabilization of the NDR region present in the intrinsic device [109, Ch. 6.2]. For large voltages, the behavior is asymptotically dominated by the load resistance, see Fig. 2.17. Although the S-NDR might be not visible in the current-voltage curve of a series connection of a thermistor and a resistor, the thermistor still exhibits S-NDR behavior, which can be revealed if its voltage drop for increasing currents is detected, separately.

3 ORGANIC TRANSISTORS

An organic transistor is an electrically switchable device using an organic semiconductor as the active material. The organic field-effect transistor (OFET) has become state-of-the art in the field of organic electronics. The OFET offers a simple geometry with a low number of fabrication steps, a high reproducibility, and is well understood. Furthermore, the variability of the employed materials has led to a continuous increase in performance over the last years. The ongoing improvements seem to have stretched the OFET already to its practicable limits, so that applications where high currents and high frequencies are required are out of the scope if one would like to preserve simple and low-cost structuring techniques. The main problem arises from the typical feature sizes in the range of 1 to 100 µm which are hampering high performance operation. Downscaling is indeed possible but would require more expensive techniques.

A promising concept is the change from a lateral charge flow to a vertical direction with respect to the substrate and the electrodes. One can easily adjust the thickness of the organic semiconductor thin films to below 100 nm within nm precision whereas the larger lateral dimensions are given by the structuring techniques. If it would be possible to employ the vertical length as the characteristic feature size of the actively operating region, a clear performance increase would be expected. This device concept can be summarized as vertical organic transistor.

In the beginning of this chapter, the OFET and its characteristics are introduced. Based on literature, different device parameters of a standard OFET are discussed. This chapter further lists current limitations of the device concept and demonstrates several solutions using transistors with a vertical alignment of the charge flow to the substrate. The developments in the field of vertical organic transistors over the last 20 years are summarized. In the end of this chapter, the focus lies on a particular approach, the vertical organic triodes (VOT), utilizing a permeable base electrode to control the current flow. The results shown in this work will rely on this device concept which will be explained by a basic operation scheme.

3.1 THE ORGANIC FIELD-EFFECT TRANSISTOR

3.1.1 Basic principle

The organic field-effect transistor is a thin film transistor (TFT) using an organic semiconductor. In Fig. 3.3, the device structure is schematically visualized. This three-terminal device has a charge injecting source (S), and a charge ejecting drain (D) contact. Due to the symmetry of the OFET, their designation only relies on the potential configuration. With the help of a third electrode, the gate (G), the current flow can be controlled. The characteristic length determining the transistor performance is the channel length L, defined as the distance between source and drain contact, typically in the range between 1 μm and 100 μm. Further, the geometry is described by the width W of the device (ca. 100 μm to 1000 μm), corresponding to the lateral extension of the channel.

Electrical switching is based on the modulation of the charge carrier density in the organic semiconductor by varying the electrical field across a dielectric material of thickness t_{diel}, ranging from 5 nm to ca. 100 nm. This gate dielectric electrically isolates the gate from the source and drain and the OFET is able to switch current in direct current (DC) mode without any gate current. The organic semiconductor layer has contact to source and drain, and allows charges to flow from one contact to the other.

In order to understand the operation mechanism in detail, one has to refer to MOS capacitors, discussed in Sec. 2.2.4, because the structures formed at the overlap area of source and gate as well as drain and gate have to be understood as such devices. As a consequence, depending on the potential configuration, the organic semiconductor can show charge depletion or charge accumulation which takes place in a very narrow zone next to the interface of the organic semiconductor and the gate dielectric. The thickness of this accumulation zone is in the range of a few monolayers of organic molecules [39]. Since the gate electrode extends into the region where no source and drain contacts are present, charge accumulation can also occur between source and drain contact, referred to as the charge channel of an OFET. In the on-state, the charge channel extends from the source to the drain contact and realizes a highly conductive path. Modulating the charge carrier density in the organic semiconductor with the help of the gate potential varies the resistance of the transistor and changes the resulting current flow over many orders of magnitude. The voltage where these effects take place is strongly related to the geometric capacitance per area of the gate dielectric, defined by

$$C_{\mathrm{diel}} = \frac{\epsilon\epsilon_0}{t_{\mathrm{diel}}} \, . \tag{3.1}$$

The accumulated two-dimensional charge carrier density can be expressed as

$$n_{\mathrm{Ch}}(x) = \frac{C_{\mathrm{diel}}}{q}\Big(V_{\mathrm{Ch}}(x) - V_{\mathrm{G}}\Big) \tag{3.2}$$

where V_{Ch} and V_{G} are the electric potential within the charge channel and of the gate, respectively. In order to reach a strong charge accumulation at low voltages, one has to reduce the thickness of the gate dielectric to a minimum without significant increase of leakage currents.

3.1.2 Device characteristics

For the theoretical description of the operation, one can draw on the theory developed for the inorganic metal-oxide-semiconductor field-effect transistor (MOSFET) [110]. However, there are some differences: Whereas both devices are unipolar, the conventional OFET solely shows charge accumulation and does not form an inversion layer of minority charge carriers. Furthermore, the organic semiconductor is intrinsic, meaning that there free charge carriers are not present except for those generated intrinsically, i.e. the layer is undoped. The type of conductivity, n for electrons or p for holes, is defined by the choice of the contact materials for source and drain [111]. Depending on the height of the electron and hole injection barrier, electron injection, hole injection, or both can be realized. However, there might be a predisposition of the organic semiconductor by having a higher charge carrier mobility for one type of charge carriers.

There are mainly three operation regimes: subthreshold, saturation, and linear. Fig. 3.2 visualizes the formation of a charge accumulation zone at the interface between the organic semiconductor and the gate dielectric. The following discussions of the electrical characteristics rely on an n-type transistor, as outlined in Fig. 3.1.

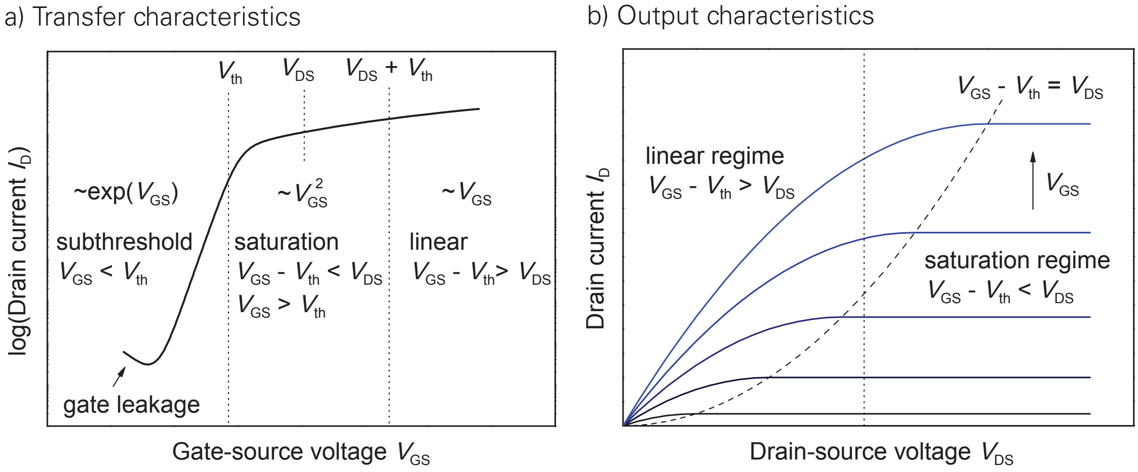

Figure 3.1: a) Transfer characteristics, showing the subthreshold, the saturation, and the linear regime in different ranges of gate-source voltage V_{GS} for a constant drain-source voltage V_{DS} (driving voltage). b) Output characteristics. The driving voltage between drain and source is varied for various gate-source voltages. For $V_{GS} - V_{th} > V_{DS}$, the linear regime can be seen, where the current increases with driving voltage. In the saturation regime, the current saturates and ideally becomes constant. The border between linear and saturation regime is indicated by a dashed line whereas a vertical dotted line is related to the transfer characteristics in a). The subthreshold regime is not visible in this linear plot due to the vanishing currents for this potential configuration.

In the subthreshold regime, no continuous charge channel between the source and the drain contact exists, as indicated in Fig. 3.2 a) and b). For a negative gate potential with respect to the source contact, the two MOS capacitors at the overlap of source and gate as well as drain and gate are biased in backward direction, so that the organic semiconductor is fully depleted (cf. Fig. 3.2 a)). Now, the transistor is highly resistive, and a residual current flow is given by a small leakage current through the gate dielectric, see Fig. 3.1 a). With increasing gate potential, a first charge accumulation arises close to the source contact and expands into direction of the drain. The current drop into the drain electrode is then given by diffusion of charge carriers rather than by a drift, and the current-voltage characteristic can be described by an exponential law for the drain current

$$I_D = I_0 \exp\left(\frac{qV_{GS}}{nk_B T}\right) \tag{3.3}$$

at a constant driving voltage where I_0 is a constant current, V_{GS} the gate-source voltage [110]. The corresponding experimental measurement is called transfer characteristic, shown in Fig. 3.1 a).

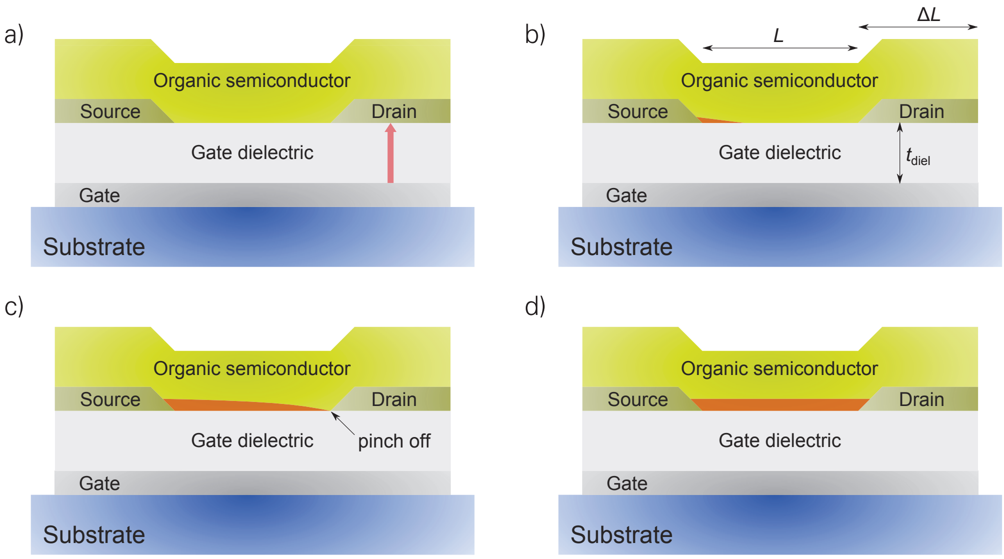

Figure 3.2: Schematic visualization of the operation states for an n-type OFET. The charge accumulation zone is indicated by an orange stripe at the interface between the gate dielectric and the organic semiconductor: a) The OFET is fully depleted and has a high output resistance, mainly determined by leakage current from gate to drain (red arrow). b) In the subthreshold regime, a first charge accumulation might occur near the source contact, but the channel does not extend to the drain contact. c) If the gate-source voltage exceeds the threshold voltage, the charge channel is almost continuously formed, but having a small pinch off zone near the drain contact, responsible for the current saturation. d) If the gate-source voltage exceeds the driving voltage plus the threshold voltage, the charge channel becomes nearly uniform and the highest conductivity for a given driving voltage is achieved.

The subthreshold regime ends if the gate-source voltage exceeds the threshold voltage V_{th} at which the channel region almost continuously connects source and drain contact (cf. Fig. 3.2). However, in this so called saturation regime, a small pinch off zone of the charge channel near the drain remains which gets larger with increasing drain-source voltage [111]. The reduced charge carrier concentration there results in a high electrical resistance and the drop of most of the electric field between drain and source. As a consequence, the current saturates, clearly visible in the output characteristics of Fig. 3.1 b), whenever $V_{DS} > V_{GS} - V_{th}$. In order to describe the current flow in this regime, one can use the gradual channel approximation, meaning that the lateral change of the charge carrier concentration in the channel region is small. Then, the electric field between source and gate is much greater than the lateral electric field in the channel

F_{Ch} [112]. The charge transport must also fulfill the current continuity:

$$j \sim q\, n_{\mathrm{Ch}}(x)^{3/2}\, \mu\, F_{\mathrm{Ch}}(x) = const. \tag{3.4}$$

and a gradually decreasing charge carrier concentration from source to drain implies an increase of the electric field at the same time, taking the charge carrier mobility μ as constant. Assuming that the charge carrier density linearly scales with the electric potential in the channel region with respect to the gate potential as given by Eq. 3.2,

$$I_{\mathrm{D}} = \frac{\mu C_{\mathrm{diel}} W}{2L} \Big(V_{\mathrm{GS}} - V_{\mathrm{th}} \Big)^2 \tag{3.5}$$

is valid in the saturation regime where $0 < V_{\mathrm{GS}} - V_{\mathrm{th}} < V_{\mathrm{DS}}$ pertains. The drain current does not depend on the drain-source voltage but increases quadratically with the gate-source voltage (cf. Fig. 3.1). For this calculation, it is further assumed that the pinch off is negligible small, and any growth of this zone does not change the current through the transistor anymore.

The gradual channel approximations applies also to the linear regime. Here, the potential configuration is described by $V_{\mathrm{GS}} - V_{\mathrm{th}} < V_{\mathrm{DS}}$, resulting into the fact that both MOS capacitors, built by the overlap of source and gate or by drain and gate, are biased in forward direction.[1] As a consequence, the charge channel does highly accumulate with charge carriers close to the source and the drain, but still exhibiting a potential drop from source to drain.

The drain current described by

$$I_{\mathrm{D}} = \frac{\mu C_{\mathrm{diel}} W}{L} \left(\big(V_{\mathrm{GS}} - V_{\mathrm{th}} \big) V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2} \right) \tag{3.6}$$

depends now linearly on the gate-source voltage and follows a reversed parabola for varying driving voltage, having zero slope at the border to the saturation regime given by $V_{\mathrm{GS}} - V_{\mathrm{th}} = V_{\mathrm{DS}}$.

Both regimes, saturation or linear, are related to strong contributions from drift currents. If contact resistances are vanishing, this could even lead to space-charge limitation effects within the channel region as described by Weis [112]. As a consequence, the gradual channel approximation has to be extended by considering a varied potential and charge carrier distribution in the channel region. However, the dependencies from the gate-source voltage as well as from the drain-source voltage given by Eq. 3.5 and 3.6 qualitatively remain the same.

3.1.3 Device geometries

There are different geometries to realize an OFET, shown in Fig. 3.3. Differences between the geometries in Fig. 3.3 lie in the arrangement of the gate as well as the source and drain contacts to the organic semiconductor layer. As a consequence, combinations of a top or bottom gate and a top or bottom contact configuration result in four variations. They differ not only in the layer sequence but also in fabrication and device performance. For example, the region where charges

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[1] Even without an overlap of source or drain with the gate electrode, the OFET still works as long as the lateral gap between the electrodes is small.

accumulate are visualized by red zones. The devices in Fig. 3.3a) and b) have contacts touching the gate dielectric and the charge channel forms in between (coplanar arrangement). Injection indicated by a red arrow is only possible at a narrow zone around the contact edge. In contrast, in OFETs where the source or drain and the gate are on opposite sides of the organic semiconductor, the charge accumulation is not only present in the channel region but extends into the overlap region of the contacts (S,D) with the gate (staggered arrangement). This allows charges to be injected at the source over a wider range, reducing the effect of contact resistance [110]. Further differences arise from the processing sequence of the layer. In a bottom gate and bottom contact geometry (cf. Fig. 3.3 a)), all steps requiring a high structuring resolution can be done with conventional lithography, so that small feature sizes can be realized. However, as mentioned above, contact resistance plays a significant role. If a top gate geometry is used, as shown in (cf. Fig. 3.3 b) and d), the gate dielectric has to be processed onto the organic semiconductor. In order to prevent damage to the sensitive molecules, one has to avoid deposition procedures where gases such as ozone, H_2O or oxygen are involved, disturbing the charge transport by either molecule degradation or by incorporating of trap or interface states. Thus, high quality dielectric layer, fabricated by atomic layer deposition, cannot be used. Other processes like sputtering or laser deposition from a material target often do not reach the layer properties required for operation at low voltages but high electrical field along the gate dielectric. Another alternative are polymer dielectric layer which can e.g. be spin-coated [113]. Thin films of this material can be processed on organic semiconductors but need layer thicknesses of the order of 50 nm to reach a suitable dielectric strength and sufficiently low leakage currents. The OFET geometry, known to reach a high performance, is shown in Fig. 3.3 c) [110]. There, a bottom gate and top contact configuration is used. The advantages are that a high quality of the gate dielectric can be achieved by processing steps which are not compatible to organic semiconductors, and the contact resistances are minimized by the staggered design. However, high resolution processing steps, like conventional lithography, are not applicable to define contacts with a short channel length. The application of shadow masks limits the feature size to above 1 µm.

3.1.4 Device parameters

Here, an overview of the state-of-the-art performance of OFETs is given. Various device parameters are discussed and compared with values achieved in literature, using data taken from experiments carried out by Klauk and coworkers found in Ref. [110]. Although there might be even better performance published as of this writing, the device presented has a repeatability, stability, and manufacturability which meets the requirements of large area production processes.

The OFET has a channel length of 10 µm and a channel width of 100 µm, realized by evaporation through shadow masks. Dinaphtho-[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) is used as the p-type organic semiconductor, reaching a field-effect mobility of 1.5 cm^2/Vs. Operation voltages are in the range of 1 V, enabling applications with low power consumption. At a driving voltage of 1.5 V, an on-state current of 15 µA is achieved and the OFET still works at 0.1 V, showing clear switching properties and a current above 1 µA. The low voltage operation arises from the gate capacitance per area of about 800 $\mathrm{nF/cm}^2$, enabling a strong charge accumulation with a charge

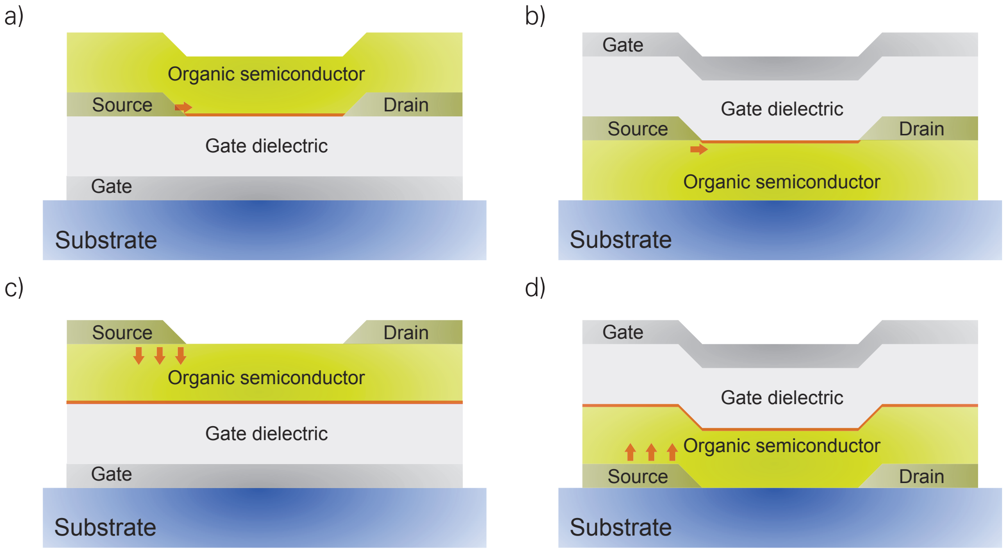

Figure 3.3: OFETs can be processed in different geometries, depending on the relative position of the contacts (Source S, Drain D, Gate) to the organic semiconductor: a) bottom gate, bottom contact b) top gate, top contact c) bottom gate, top contact d) top gate, bottom contact. The red zone indicates the charge channel, developing in the on-state (strong accumulation) and the arrows injection of charges at the source contact.

carrier density per unit area of $1.3x10^{13}$ cm^{-2} at 1 V which corresponds to a charge carrier density per unit volume of $4.7x10^{19}$ cm^{-3}.

Current density The current of an OFET scales with the width of the contacts but does not scale with the active area between the source and the drain contact. A characterization of the device by a mean current density, given by the total current and this area does not make sense. However, one can estimate how much current is flowing per area, occupied by the transistor, to enable a comparison with vertical organic transistors. In principle, the active area of the OFET is given by the product of channel length and the channel width but also the size of the contact has to be taken into account leading to the total footprint area. It can be assumed that the length of the contacts will be of the same size as the channel length due to the characteristic length of the structuring process. Thus, the minimum area of the transistor discussed here is about 100 µm x 30 µm and considering the current flow of 15 µA, a current density of about 500 mA/cm^2 is achieved [110].

Such a current per occupied area can be also derived from the theory of the OFET. Assuming an on-state at a gate-source voltage fulfilling $V_{\mathrm{GS}} - V_{\mathrm{th}} = V_{\mathrm{DS}}$, one can derive independently of the saturation regime (s. Eq. 3.5) or the linear regime (s. Eq. 3.6) the following equation

$$j_{\mathrm{OFET}} = \frac{\mu C_{\mathrm{diel}}}{6L^2} V_{\mathrm{DS}}^2 \tag{3.7}$$

where the area $A = 3LW$ is estimated as above. Now, the current density does not depend anymore on the channel width and it becomes clear that achieving higher values is strongly related to a reduction of the characteristic feature sizes of the device, here given by the indirect proportional dependence on the quadratic channel length L. For example, at a channel length of 1 µm, a current density of ca. 45 A/cm^2 would be possible, using the parameters from above.

Transconductance A similar estimation can be done for the transconductance per footprint area A of the transistor

$$g_{\mathrm{m,OFET}}/A = \frac{\mu C_{\mathrm{diel}}}{3L^2} V_{\mathrm{DS}} \tag{3.8}$$

using the considerations above. Typically, the transconductance of an OFET is normalized to the channel width in order to compare with other lateral geometries. However, to make a realistic comparison with the vertical organic transistor developed in this work, properties have to be scaled to the area they occupy. Then, the reference OFET discussed here achieves a transconductance per area of 500 mS/cm^2 using the experimental value of 15 µS or 600 mS/cm^2 by using Eq. 3.8

On/off ratio and current gain A parameter which is highly relevant for applications is the on/off ratio, describing the factor between the current flow in the on and in the off-state. The on/off ratio should be as high as possible to drive large currents in the on-state, stop the operation of connected devices in the off-state, as well as to minimize the power consumption in the off-state. Whereas the on-state is limited by the geometry and the charge carrier mobility of the organic semiconductor, the off-state is mostly determined by gate leakage current, flowing to the drain. A state-of-the art OFET reaches eight orders of magnitude on/off ratio, sufficiently high for industrial requirements [110]. In contrast, the current gain of an OFET is seldomly discussed. The reasons are that the device principally switches without gate current and the ratio between drain and gate current I_C/I_G is given by the leakage current, flowing from the source to the drain. A standard OFET easily reaches five orders of magnitude current gain [110].

Subthreshold swing In order to characterize the transition from off- to on-state, the subthreshold regime is characterized by the subthreshold swing

$$S = \frac{nk_B T}{q} \ln(10) \quad , \tag{3.9}$$

describing the change in gate potential necessary to vary the drain current by one decade. The ideality factor $n > 1$, introduced in Sec. 2.2.4, originates from trap states at the interface between the organic semiconductor and the gate dielectric. For $n = 1$, a minimum subthreshold swing of 60 mV/decade is possible at room temperature. Nowadays, OFETs reach 80 mV/decade, being close to ideality [110].

Transit frequency As a last parameter, the transit frequency, reached at unity current gain $I_C/I_G = 1$, is discussed here. The related switching speed of the device strongly determines the range of operation. The transit frequency of an OFET

$$f_T = \frac{g_m}{2\pi C_{\mathrm{diel}} W(L + 2\Delta L)} \tag{3.10}$$

is related to the area where charges accumulate at the gate dielectric and the transconductance g_m, determining how fast the capacitance can be charged [110]. Besides the channel width W and the channel length L, the overlapping distance ΔL (cf. Fig. 3.2b)) between gate and source/drain determines the total capacitance. An estimation of the transit frequency can be done by assuming operation in the linear regime and setting $\Delta L \sim L$ because both lengths will be again determined by the structuring technique. Then, it reads

$$f_\mathrm{T} = \frac{\mu}{6\pi L^2} V_\mathrm{DS} \tag{3.11}$$

and it becomes obvious that the transit frequency depends inversely proportional to the square of the channel length and can be linearly increased by the drain-source voltage (cf. Ref. [114]). Using the parameters from above, a unity current gain is estimated to be at 80 kHz at a driving voltage of 1 V. For comparison, a ring oscillator based on OFETs with $L =$10 µm and a mobility of 1.5 $\mathrm{cm^2/Vs}$ has resulted into a transit frequency of 25 kHz at a circuit driving voltage of 3 V [110]. As a consequence, OFETs with a low resolution feature size, operating at low voltages are not able to reach high-frequency operation in the Megahertz region. However, by downscaling the channel length to 1 µm, operation at 2.2 MHz in a ring oscillator has been demonstrated at a driving voltage of 4.2 V [115].

3.1.5 Issues of OFETs

In order to understand the current limitations of OFETs, several aspects influencing the device performance will be discussed here. Nevertheless, there are also several approaches to overcome these issues, and their advantages and disadvantages are also discussed.

Contact resistance The transconductance of an OFET is typically determined by the charge transport through the charge channel. This is valid for devices with a large channel length, depending on the charge carrier mobility. However, by shrinking down the dimensions of the OFET, the contact resistance plays an increasing role, meaning that at larger currents, a significant electric field drops at the contact between source and the organic semiconductor [114, 116]. As a consequence, the transconductance of an OFET is limited by charge injection instead of charge transport. Since the contact resistance does not scale with the dimensions of the channel length, the scaling laws for transconductance, current density, and transit frequency do not apply anymore. In particular, the measured charge carrier mobility, assuming an unimpeded operation in saturation or linear region, decreases with downscaling of the dimensions [117, 118]. A performance increase by a reduction of the channel length is then out of reach. In general, the effect becomes more important the higher the charge carrier mobility of the organic semiconductor is [119].

The standard procedure to minimize the effect of contact resistance is the reduction of the charge injection barrier at the source contact either by molecular doping, proper choice of contact materials, or the usage of self-assembled monolayers (SAM), introducing an energetic shift at the injection interface [70, 120, 121]. Drawbacks are that doped layers have to be structured with the source and the drain contact to prevent leakage currents, flowing from source to drain, so that this method is not compatible with prestructured electrodes in a bottom gate, bottom contact configuration based on conventional lithography. By using top contacts, the layers enhancing the charge injection can be processed e.g. by shadow mask with the same mask as the source and drain mask but are likewise hampered by the reachable feature sized of the structuring techniques. In contrast, SAMs are applied from solution, attaching the surface of the source and drain contacts and thus are only relevant for a bottom contact configuration. Adapting the contact by changing the electrode material has the disadvantage that either a certain contact resistance remains or only a particular combination of contact material and organic semiconductor works.

Structuring techniques The most critical limitation and at the same time the most fertile prospect lies in the characteristic feature size which can be reached by a particular structuring technique. It has been shown that OFETs can be fabricated with channel length below 100 nm [122]. For that purpose, e-beam lithography, photolithography, shadow deposition, underetching, nanoimprinting, rubber-stamping, or micro-contact printing have been used [123]. However, these methods have at least one of the following disadvantages: being cost expensive, having a low throughput, unemployable on large area, or just fitting to only a single gate and contact configuration. In contrast, evaporation through shadow masks does not have the drawbacks mentioned above, but is also hampered by some aspects. Sheet metal masks can be purpose-built for new designs and applications, at a minimum of cost. They are typically fabricated by laser cutting, but the minimum feature size is limited to the range of 10 µm. Smaller dimensions can be reached by polyimide shadow masks or high resolution stencil masks, having the drawback that they are not reliable on large area related to the stability of the tiny features within the mask [124]. A suitable approach consists in a lithography compatible with organic materials allowing for structuring of top contacts on the organic semiconductor layer of an OFET [125, 126]. The progress in this field is now at the beginning, and the demonstration of a sub-µm channel length OFET with low contact resistance, operating at high-frequency is still pending. However, further investigations might lead to an interesting alternative to shadow mask deposition.

Parasitic overlap capacitance As already discussed for the transit frequency, an overlap exists between source and gate as well as between drain and gate which can reduce the switching speed of the transistor. Zaki *et al.* figured out that the overlap between source and gate has a much stronger influence on high-frequency operation than the gate and drain overlap [127]. For example, decreasing the source-gate overlap from 7 µm to 1 µm and simultaneously increasing the drain-gate overlap improves the transit frequency by a factor of two. As a consequence, it is not sufficient to downscale the channel length if the overlap between the contacts and the gate remains large. A technical solution to overcome this problem are self-aligned gate or source and drain electrodes [128]. For that purpose, an already deposited electrode acts as a light opaque mask, so that in a subsequent lithography step, the following electrodes can be perfectly aligned. This method even allows to prevent any electrode overlap. However, a certain overlap between source and gate has the advantage that injection takes place over an extended range at the source contact, so that the measured contact resistance is minimized [118].

Short channel effects By downscaling the channel length, the gradual channel approximation might not be valid anymore. This is the case if $L < 20\,t_{\mathrm{diel}}$, so that the electric field between source and gate cannot be assumed to be large in comparison to the electric field between source and drain [122]. Then, short channel effects such as a vanishing current saturation can be observed for the output characteristics. This also implies that the subthreshold regime is no more independent from the driving voltage which can be interpreted as a threshold voltage shift [114]. As a consequence, these deviations from the ideally described transistor behavior have to be considered by the circuit design. Especially, the arising dependence on the driving voltage in the saturation regime means that both the gate-source voltage as well the drain-source voltage have to be adjusted correctly in order to achieve the desired current output, e.g. for driving a display pixel (cf. Ref. [129]).

3.1.6 Outlook

At the moment, the main attempt for device improvement besides downscaling the dimensions is to optimize the charge transport. Many investigations deal with the enhancement of the charge carrier mobility of the organic semiconductor by increasing its crystallinity and thus reducing grain boundaries between neighboring crystallites which may form charge traps disturbing the current flow [130]. One possibility is the use of single crystals, completely covering the charge channel [131]. This approach is applicable for a single OFET but it reaches its limits for large scale production, so that the corresponding investigations mainly address the basic physics of charge transport in OFETs. However, there are new fabrication methods such as solution-sheared organic semiconductors, recrystallization from solution, or off-centre spin-coating [26, 132, 133]. By these methods, outstanding average charge carrier mobility of more than 10 cm^2/Vs have been obtained for devices with rather large channel length of 50 to 100 µm. The future may reveal whether this record performance can also be obtained at low channel length when contact resistances play a major role. A more comprehensive overview of the current progress in the field of OFETs has been recently given by Henning Sirringhaus [116].

Despite several limitations mentioned in this section, OFETs have reached a competitive performance. For example, thin film transistors (TFT) based on amorphous silicon have a charge carrier mobility around 1 cm^2/Vs and are already employed for the active matrix backplane of liquid crystal displays as well as OLED displays [110, 130]. Thus, OFETs having similar or even higher charge carrier mobilities should be able to perform the same task as long as the prerequisites like reliability and stability are fulfilled [129]. One difference to inorganic TFTs might be of course that smaller channel lengths can be reached by conventional lithography, and contact resistance can be easily avoided by contact doping [119]. Nevertheless, if the best results obtained for OFETs can be made available in industrial production, even polycrystalline silicon with ca. 10 cm^2/Vs can be eventually replaced [110].

3.2 OVERVIEW OVER VERTICAL ORGANIC TRANSISTORS

The last section showed that downscaling the channel length is the most promising way to achieve higher currents, transconductance, current per area, and switching speed. Whereas the lateral dimensions are often limited to the µm range, in vertical direction, layer thicknesses can easily be defined in the nm range by evaporation of the materials. Thus, changing from a laterally oriented charge channel to a vertical one is a viable solution to realize short channel transistors. The challenge consists of finding appropriate geometries, processing techniques, and physical effects which allow to control the current flow in vertical direction without relying on time- or cost-intensive methods. Such transistor structures are referred to as vertical organic transistors. They can operate at low voltages and have layer thicknesses of the electrodes and the organic semiconductor in the range of 100 nm.

Scientific work in this field can by mainly classified into four different approaches. They differ from each other by their layer arrangement, their structuring techniques, and their working mechanism. In this section, each approach is introduced and representative achievements are discussed. Following this, the effort spent on this topic is finally summarized by discussing the scientific output in the last years.

3.2.1 VOTs with an unstructured base electrode

Working mechanism One way to build a vertical organic transistor is to stack three metallic or highly conductive electrodes in a sandwich geometry, separated by an organic semiconductor layer. The layer sequence is visualized in Fig. 3.4. The middle electrode is very thin with a thickness in the range of 10 to 15 nm and allows charge carriers to be transmitted through it. Thus, if charges are injected into the organic semiconductor at the top electrode, they can reach the bottom electrode by a transmission through the base electrode without reaching electrodes Fermi level. The electrode of the triodes are named emitter, base, and collector, which strengthens the similarity of this device to the bipolar junction transistor (BPT) having a similar scheme of the current flow. A potential drop between base and emitter leads to charge injection at the emitter. Only a small part of this current drops into the base (I_B) and has to be conducted away in order to keep the base potential constant. The major part of the emitter current I_E reaches the collector (I_C), so that a current amplification of $I_C/I_B > 1$ is achieved.

There are two concepts to explain the function of such a transistor with a thin but unstructured base electrode. If the thin base electrode forms a continuous and conductive layer after deposition, charge transmission can only be explained by ballistic transport through the base electrode. This device concept has been introduced by Atalla and Kahng as well as by Geppert in 1962, and the corresponding transistor is called metal-base transistor (MBT) or hot-electron transistor [134, 135]. The latter designation arises from the fact that e.g. electrons reaching the base electrode from the emitter side have a higher energy than electrons at the Fermi level of the base electrode, according to the energy of the transport level in the semiconductor layer. If these electrons enter into the base electrode, they appear as 'hot' because at thermal equilibrium, high temperatures would be necessary in order to have a significant amount of electrons at energies

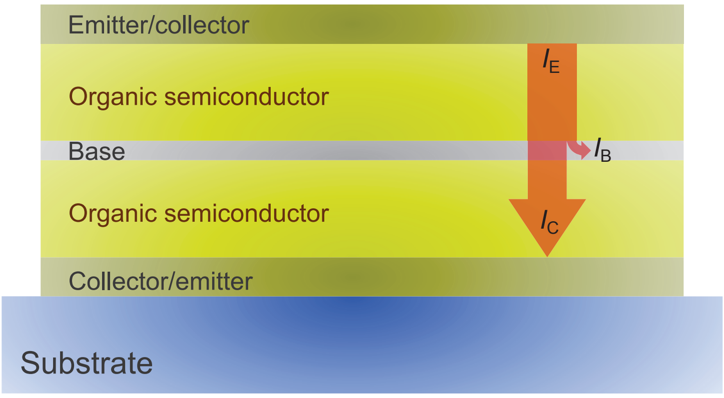

Figure 3.4: Schematic structure of VOT with an unstructured base electrode which is very thin (10 - 20 nm) in order to allow for charge carrier transmission

well above the Fermi level as described by the Fermi-Dirac statistic. One can describe the transport in the metallic base as a coherent ballistic transport from a semiconductor Bloch state at the emitter side of the device to another semiconductor Bloch state on the collector side. Ideally, both states have the same energy. The probability for a successful charge transmission is given by the transmission factor[2]

$$\alpha = \alpha_0 \mathrm{exp}(-t/L_\mathrm{B}) \tag{3.12}$$

which decays with the base thickness t and the mean free path L_B of the hot-electron, resulting from phonon, electron-electron, electron-defect, and electron-impurity scattering [136]. α_0 is the maximal reachable transmission determined e.g. by optical phonon-scattering in the emitter and the collector layer. Further, the quantum-mechanical transmission at the collector exerts an influence due to possible reflection of the charge carrier at the energy barrier between the base and the collector layer. For example, for Si/Au/Si layer structures, Crowell and Sze have observed an α_0 of 0.37 and a L_B of 229 Å at room temperature. These values demonstrate that this type of charge transmission process is accompanied by a strong loss of charge carriers into the base electrode and thus a low current gain. Several investigations show that the transmission factor does not exceed 50% [137–139] and thus the current gain remains below 1, which probably has led to the limited interest in this type of device. However, it has been possible to increase the transmission factor to 91% by using a higher energy barrier between base and emitter than between base and collector. As a consequence, even charges already scattered in the base might have enough energy left to reach a state in the collector. Further improvement was also achieved by inserting oxide layers next to both sides of the base electrode, improving the tunneling probability from the emitter to the collector to above 90% [139, 140]. In recent times, the device concept enjoys a revival in form of the graphene base hot-electron transistor [141–143]. Due to use of graphene as the base electrode, the length for ballistic transport is reduced to a minimum. The transmission factor is still low, not higher than 10%, but the short transit time through the graphene base makes the device a promising candidate to achieve THz operation [144].

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[2] Often also called transport factor or common-base current gain.

Another approach explaining the charge transmission through the unstructured base electrode consists in a permeable base transistor (PBT). A grid electrode unintentionally forms during the deposition step, acting as the base and allowing charges to be transmitted through their openings. For example, in 1985 Hensel *et al*. demonstrated a Si/$CoSi_2$/Si transistor [145, 146]. The 10 nm metallic $CoSi_2$ acts as the base and controls the charge flow between the upper and the lower Si layer. Later, it has been shown that the $CoSi_2$ layer, epitaxially grown on Si, exhibits pinholes with a lateral mean diameter of 200 nm [147]. The transistor had a charge transmission above 95%, decreasing to a lower percentage for an almost pinhole free base layer [138, 147]. Here, it should be noted that the original concept of the PBT has been proposed by Bozler and Alley in 1980 for a device with a predefined grid electrode, and it will be discussed in more detail in the following section 3.2.2 where VOTs with a structured grid electrode are discussed [148].

Literature overview Since no sub-μm structuring of the base is required, the concept of a transistor with an unstructured base electrode has drawn a lot of attention in the field of organic electronics. As depicted in Fig. 3.4, organic PBT (OPBT) or organic MBT (OMBT) are usually built by inserting a thin metallic layer between two organic semiconductor. Up to now, many groups worldwide published device structures, showing clear charge carrier transmission [10, 11, 149–200]. The working mechanism is controversially discussed and often the experiments carried out do not allow for an unambiguous statement whether the charge transmission is attributed to pinholes, ballistic transport, or tunneling. However, recent publications of So and coworkers as well as by this work led to an understanding of the VOT as a PBT with a nano-porous base electrode, unintentionally formed during the deposition of thin metal films on rough organic semiconductor layers [182, 199]. This hypothesis is supported by the bidirectional operation of the devices and transmission electron microscopy of the base electrode for particular material systems. Nevertheless, it remains unclear whether these results can be adopted to similar device structures.

Due to the large amount of scientific work on this topic, here it will be the aim to shortly summarize different representative results. The first work using organic semiconductors has been carried out by Yang and Heeger in 1994 who developed a polymer grid triode by using a grid-like and conductive polymer network [10]. McElvain *et al*. analyzed and optimized this device structure, reaching current densities of 1 mA/cm^2 at a driving voltage of 5 V, but the on/off ratio remained below 10 [150, 151]. Starting from 1998, Kudo and coworkers developed VOTs based on the system CuPc/Al/CuPc [152–154]. They achieved operation at 2 V, having current densities of about 1 mA/cm^2 and an on/off ratio of more than two orders of magnitudes. A promising work appeared in 2005 by Fujimoto, Nakayama, and Yokoyama [11]. They used the layer system Me-PTCDI/Al/C_{60} and exposed the base to air. For the first time, a VOT with an unstructured base electrode achieved a high current gain above 100. Further, the current density at an operation voltage of 5 V exceeded 300 mA/cm^2. In the following years, several optimizations of this device structure, leading e.g. to on/off ratios greater than 10^5 by heat treatment of the base electrode in air or to current densities close to 1000 mA/cm^2 at a driving voltage of 7 V have been made [156, 168, 172, 174]. Also light-emitting devices have been demonstrated by embedding OLEDs into the layer [165, 179]. A similar device structure has been investigated by Cheng *et al*. who uses a CuPc/Al/NPB/CuPC layer sequence based on the preliminary results of the Kudo group mentioned above [161]. First published in 2007, at a driving voltage of 6 V, they achieve a current density of 2.5 mA/cm^2 and a current gain of 1.9. Later, the bottom layer has been exchanged by pentacene, resulting in a current density of ca. 10 mA/cm^2 at a driving voltage of 5 V as well as an on/off ratio of 10^3 [170, 187]. The device operation has been further demonstrated in an inverter circuit, working at 4 V [169, 175].

Despite the progress for VOTs with an unstructured base electrode, the achievements stay behind the expectations for a short channel device. For example, the measured switching speed remains restricted to the lower kHz range [165, 170]. Up to now, the performance of the VOTs cannot compete with a standard OFET in terms of driving voltage, current density, current gain, and on/off ratio, compare Sec. 3.1.4. However, it will be shown by this work that the device operation can be clearly improved, satisfying the expectations arising from the concept of this short channel transistor.

Advantages and disadvantages The main advantage of a VOT with an unstructured base electrode is the simple realization by subsequently depositing several layers through shadow masks. This 'sandwich'-geometry of the device also allows to stack other devices on top or underneath, e.g. an OLED, which is beneficial for a high integration density. Furthermore, it is possible to insert a layer, modifying the contact resistance of the emitter contact, just by processing through the same shadow mask as used for the electrodes. Drawbacks are that this design concept is momentarily less understood, so that it is difficult to estimate the limitations of this technique, especially regarding the switching speed and the current densities. It might also be hampering that there is only a handful of published material combinations for the layer system which show a current amplification. Currently, it is unclear in which way conclusions can be adopted to another device structure or in which way materials can be exchanged. Nevertheless, the simplicity of this concept makes this approach very interesting for further investigations of short channel devices, and it will be part of this work to shine light on the prospects and challenges of this device concept by resolving the limitations mentioned above.

3.2.2 VOTs with structured base electrode

Working mechanism As discussed for VOTs with unstructured base electrode, device function is limited to a small number of material systems. However, if the base electrode is intentionally structured with openings of a defined size, the working mechanism can be clearly attributed to a permeable base transistor [148]. A schematic view on the device structure is given in Fig. 3.5. Again, the device consists of outer electrodes as emitter and collector as well as a middle base electrode. The openings in the base should be large to guarantee a large charge flow, but small enough to keep control over the current by the base potential. Typically, the size of the opening $w_{\text{opening}} \sim 100\,\text{nm}$ is in the range of the total layer thickness. In the on-state, the current flow is limited by space charges under the assumption that the contact resistance at the emitter has been reduced to a minimum. The transistor can be switched off by applying a base potential which leads to a potential maximum in the openings (saddle point) as well as a reduced electric field at the emitter contact, hindering charge injection. Since there is no charge accumulation zone, necessary for the device function, the base electrode can be completely separated from the emitter by a thick insulating layer (cf. Fig. 3.5). As a consequence, charge flow from the

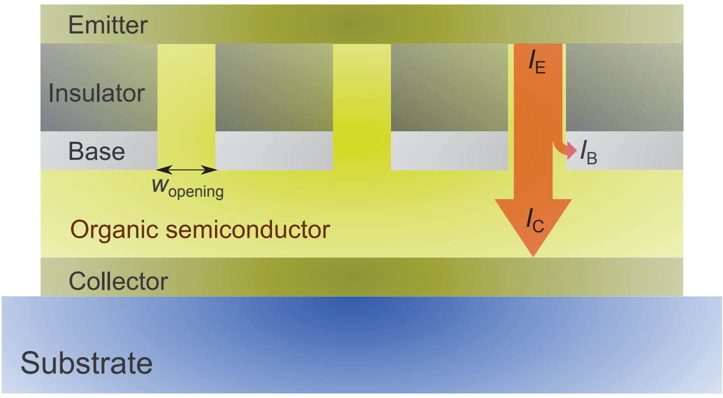

Figure 3.5: Schematic structure of a VOT with a structured base electrode. The openings in the base electrode have a size in the range of the total thickness of the organic semiconductor or lower in order to be able to suppress the current flow from emitter to collector by the potential at the base.

emitter into the base decreases and the current gain increases. Principally, such an insulating layer could also be inserted between the base and the collector in order to suppress leakage current in the off-state.

Having a grid electrode, the PBT shows similarities to a vacuum tube triode [201]. Both devices have an emitter (cathode), base (grid), and a collector (anode) electrode, and the working mechanism is based on the punch-through of the electric field through the opening, efficiently conducting charges from one side to the other side of the grid electrode. In that way, a PBT can be understood as a miniaturized vacuum tube where the vacuum is replaced by a semiconducting material with the advantage that due to the improved injection of charge carriers at the emitter and the smaller dimensions, much lower operation voltages can be achieved.

The device concept of a PBT has been first time proposed by Bozler and Alley in 1980 [148]. As the base, a lithographical structured metal electrode is used, having lateral dimension in the sub-µm range. Due to the low resistance of the electrodes and the low capacitance between the contacts, the PBT has been discussed as a fast switching transistor, reaching frequencies in the range of 10 to 100 GHz [202]. A similar device is called the static induction transistor (SIT) [203]. The main difference to the PBT is that instead of a metallic electrode, highly p- or n-doped regions are used to control the charge flow. Whereas for a PBT, the leakage current from emitter to base is given by the forward direction of a Schottky diode, the SIT forms a pn-junction which determines the current flow into the base.

Literature overview In many works, this concept has been adopted to organic semiconductors [162, 204–251]. Starting from 2000, Kudo and coworker published transistors referred to as organic static induction transistor (OSIT) [204–206, 208–210, 212, 215, 216]. However, due to usage of a metallic grid electrode it should rather be declared as a PBT. They use a strip-like shadow mask to realize a structured base electrode with a stripe periodicity of 40 µm. As a consequence, they have two complementary problems: Either the opening is small but there is a large leakage current flowing from the emitter into the base, or the openings are wide, so that the current flow cannot be controlled anymore [209]. After they inserted insulating layers next to the base electrode, the gate leakage has been reduced, but the current density and the on/off ratio remained rather low [233].

In 2006, Chao et al. demonstrated a PBT with a base structured by polysterene spheres [217]. This technique allows to realize openings with a diameter in the range of 100 nm to 500 nm distributed all over the active area. Later, they inserted an insulating layer underneath and above the base electrode to decrease the leakage currents [226, 232]. Furthermore, they optimized the distribution of the polysterene spheres by making them more uniform over the substrate [243]. Improved devices show current densities above 10 mA/cm^2 at a driving voltage of 1.5 V and a good bias stress stability [249]. They exhibit on/off ratios of 4 to 5 orders of magnitude and a current gain similar to OFETs [235, 242]. With a subthreshold swing of 96 mV/decade the performance is close to the optimum value of 60 mV/decade. Although the device concept is promising for high-frequency operation, no such measurements have been presented, yet.

Other structuring techniques which have been successfully employed by are laser interference lithography, nanoimprint lithography, micro-contact printing and electron beam lithography [241, 244, 245, 247, 250].

Advantages and disadvantages Although the main advantage of VOTs with a structured base electrode is expected to be high-frequency operation, no related results have been published so far. Nevertheless, the possibility to reduce the electrode resistance to a minimum and the low capacitances in the device due to the absence of a charge accumulation region makes this device the ideal candidate to reach switching speeds similar to the performance achieved for organic diodes [56, 252, 253]. Therefore, the usage of insulating layers above and underneath the base electrode is beneficial to reduce leakage currents as well as geometrical capacitances. Further advantages include the possibility to easily modify the contact resistance by insertion of injection layers and the capability to stack with other devices. Furthermore, the device geometry can be well adjusted by most of the structuring techniques, allowing for modeling and optimization by simulations.

Problems might arise if the size of the openings is too large, leading to poor control over the current flow. The feedback of the electrical field from the collector onto the emitter further implies that currents do not saturate in the on-state or only show saturation if one accepts a reduced on-state current [244]. In the future, it has to be shown that structuring methods are compatible with large areas and industrial processing standards. For example, methods using polysterene spheres must result in a homogeneous and repeatable device performance which still has to be proven. One drawback might be that the best devices reach current densities between 10 mA/cm^2 and 100 mA/cm^2, and thus they cannot compete with standard OFETs. At the moment, the polymer P3HT is widely used as the organic semiconductor. However, if it will be possible to exchange it by a material with a higher charge carrier mobility, a clear performance increase can be expected, making these devices interesting for amplifier applications at high frequencies.

3.2.3 Charge injection modulating transistors

Working mechanism The previously discussed transistors are based on a middle electrode, controlling the charge flow. However, new device concepts called vertical organic field-effect transistor (VOFET) have appeared in literature recently. One of them is a device where the charge injection at a source electrode can be controlled by the modulation of an electrical field at its edge. In order to distinguish different trends, this transistor is named here charge injection modulating transistor (CIMT). The structure is presented in Fig. 3.6, consisting of a capacitor and an organic diode with a common perforated source electrode. A gate dielectric between the gate and the source electrode forms the capacitor, whereas the organic semiconductor forms the organic diode with the help of the source and the drain electrode. Due to the openings in the source electrode, the potential at the gate electrode can penetrate and influence the electric field around the source electrode. Especially, at the edges of the source electrode, a strong electric field enhancement occurs which is able to significantly influence the charge injection at this electrode [254]. The effect only takes place along the edges of the openings, determining the region where a current flow contributes to the overall device current (active region). In contrast to that, there are non-active regions of the source electrode where no field modulation by the gate is possible. These regions are located away from the edges and are necessary to ensure a sufficiently high conductivity of the source electrode. For a constant driving voltage between source and drain, the charges injected in these non-active regions flow independently from the gate potential. As a consequence, any charge injection into the non-active region leads to poor off-state conditions. In order to circumvent that problem, one has to ensure the presence of a large Schottky-barrier at the interface between the source contact and the organic semiconductor. Then, a small current will flow in the off-state, but it can be strongly increased by the gate-controlled electric field enhancement at the edges, leading to a Fowler-Nordheim tunneling as the dominant injection process [255]. Finally, this might lead to a charge accumulation in the opening due to the electric field dropping over the gate dielectric [256]. Between this zone rich in charge carriers and the drain contact, a potential and charge concentration gradient develops which transports charges by drift and diffusion to the drain. In principle, this device can be understood as a switchable diode since the source contact can be modulated from Schottky to Ohmic. Sometimes the switching of the injection is also referred to as a work function modulation in the source electrode by the gate potential [254, 257]. This might be the case for very thin metallic layers or electrodes having a low number of free charge carriers, so that external electric fields are not fully screened.

An analog device concept can be found for inorganic semiconductors, called Schottky-barrier transistor or Schottky-barrier MOSFET [258–260]. There, in a lateral field-effect transistor geometry, the contact resistance at the source contact is modulated by the gate potential for a short channel device. Similar effects have been found in OFETs having a double-gate architecture which allows to enhance the electric field at the source contact and thus manipulate the contact resistance [261].

Literature overview The field of CIMTs is becoming increasingly active over the years [254–257, 262–288]. The publications referenced above solely deal with organic molecules as the semiconductor and the work of some pioneering groups is presented in the next paragraphs.

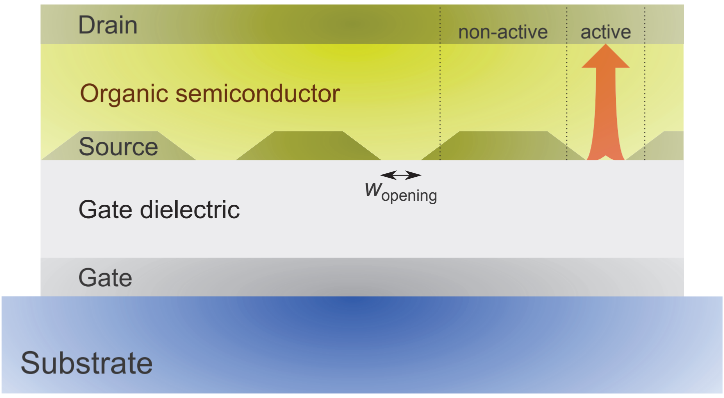

Figure 3.6: Schematic structure of a charge injection modulating transistor. The openings of the source electrode allow for the punch-through of the electrical field, leading to an enhancement of the electrical field at the edges of the source electrode in the on-state, increasing the charge injection. Further, the gate potential might be able to influence the work function of the source and thus the charge injection barrier at the interface to the organic semiconductor.

The first CIMT using an organic semiconductor has been realized was in 2004 by Ma and Yang [262]. They showed a transistor consisting of a capacitor cell using LiF (gate dielectric), a Cu source electrode, and C_{60} as the organic semiconductor. Although no sub-μm structuring is used for the source electrode, a clear switching of the transistor is present. It is argued that the deposition of a metal onto a rough layer of LiF leads to a non-continuous growth of the source electrode, so that small pinholes allow for the punch-through of the electrical field [264, 265]. At a driving voltage of 4 V, a current density of 4 A/cm^2 and an on/off ratio of less than 5 orders of magnitude are specified by the output characteristics. However, at the same time, they present a gate sweep where the same device does not reach more than 400 mA/cm^2 at exactly the same potential configuration, but now the on/off ratio is about 6 orders of magnitude [262]. After two more publications appeared in 2007, which were not able to repeat the highest current densities, no more work on this topic has been demonstrated by this group [264, 265]. One reason might be the fact that the capacitance of the LiF capacitor strongly varies with humidity, changing by two orders of magnitude. Even though the results have to be treated with caution, the outstanding performance achieved in their first publication has triggered a series of works on this topic and can be seen as the starting point of investigations on vertical organic field-effect transistors. The last time that a CIMT has been reported, using a gate dielectric with a very high capacitance per area and a non-structured source electrode was in 2010 by Jiang and coworkers [269]. They reached at a driving voltage of 0.8 V, a current density of 1.0 A/cm^2, a subthreshold swing of 80 mV/decade, and an on/off ratio in the range of 6 orders of magnitude. Despite the promising results, no further publication appeared by this group as of this writing.

A continuous progress and output has been achieved by the group of Nir Tessler, mainly carried out by Ariel J. Ben-Sasson [256, 268, 275, 276, 279, 280, 284]. The device concept is named by them as patterned electrode vertical FET (PE-VFET). Starting from 2009, their research is based on the structuring of a thin metal electrode by a block copolymer nanotemplate [268]. By the help of this technique, a good coverage of openings within the source electrode can be achieved, and the diameter of the circular openings is nearly constant over the active area, e.g. 80 nm [280]. At a driving voltage of 3 V, an optimized device reaches current densities above 10 mA/cm^2, an on/off ratio about 10^3, and a subthreshold slope of 1.5 V/decade [283]. Higher current densities than 100 mA/cm^2 are possible, but are accompanied by driving voltages of more than 5 V [279]. In 2013, Greenman *et al*. demonstrated switching from off- to on-state within 2 µs and reached a current density of 3 A/cm^2 at a driving voltage of 20 V. If one compares with the OFET described in Sec.3.1.4, it must be stated that in terms of current density and low voltage operation, the lateral transistor device still performs better. However, the switching speed is faster in comparison with OFETs having 10 µm channel length.

Finally, the work of Andrew Rinzlers group is presented here [254, 255, 267, 270, 271, 273, 274, 281, 282]. Due to a strong expertise with carbon nanotubes (CNT) [289], conductive sheets of this materials are employed as the source electrode of the transistor. The corresponding device concept is called carbon nanotube enabled vertical organic field-effect transistor (CNT-VOFET) and the first working device has been presented by Liu *et al.* in 2008 [267]. As a typical feature of the CNT network, openings form between the bundles of CNTs, enabling the punch-through of the electrical field from the gate necessary to control the charge injection at the surface of CNT electrode into the adjacent organic semiconducting layer. After optimizing the capacitance of the gate dielectric, in 2010 McCarthy *et al.* were able to demonstrate a transistor working at 3 V with current density of 110 mA/cm^2 and an on/off ratio about 10^5. The subthreshold slope was limited to be 500 mV/decade due to the fact that a countervoltage had to be applied to the gate in order to suppress a residual charge injection at the source contact. Nevertheless, this has not been an obstacle to realize CNT-VOFETs with stacked OLEDs on top, showing red, green, and blue light emission at a display-relevant brightness, using a total driving voltage of less than 7 V [274]. Nowadays the technique is considered by them for use in OLED displays [282]. A second approach has been pursued by this group, employing graphene as the source electrode [281]. It has been shown that even without any openings in the material, a clear current switching by more than three orders of magnitude can be obtained, explained by the modulation of the work function of graphene by the gate potential. However, if the graphene electrode has been perforated, a clear increase in on-state current density by two orders of magnitude has been found, contributed to the electrical field enhancement at the edges of the openings [254, 281]. The effect of modulating the charge injection barrier by the gate potential has also been investigated by other groups, calling their device a graphene barristor [183, 286].

Advantages and disadvantages Clear advantages of this device concept are a high current gain due to the insulating gate dielectric, the possibility to stack with other devices, and no need for doped layers, simplifying the layer stack since the injection of the contact itself is modulated. The working mechanism allows further to realize p- and n-type devices. In principle, it is even possible to integrate both operation modes into one device if the electron and the hole injection barrier of the source electrode to the organic semiconductor are equal [264]. Then, the polarity of the charge carriers could be adjusted by the drain potential.

Drawbacks are that the source electrode is mostly deposited on the gate dielectric, acting as a substrate, so that inverted structures interesting for stacking on top of OLEDs are difficult to realize. There are individual publications demonstrating very high current densities above 1 A/cm^2, but the reproducibility has to be proven. Most works reach current densities in the range of 100 mA/cm^2 if low voltages are considered. Furthermore, the operation is limited to particular material combinations of the source electrode and the organic semiconductor. Only with a pronounced Schottky-barrier high on/off ratios can be achieved. It will also be of interest whether the structuring techniques used to perforate the source electrode are compatible with large area processing. Nevertheless, most structuring techniques are relatively easy to use and show reproducible results, so that such charge injection modulating transistors can be fabricated with minimum effort.

3.2.4 Vertical organic field-effect transistor

Working mechanism A second approach to build a VOFET is a vertical organic transistor which can be understood as a staggered OFET with the drain electrode shifted above the source electrode. The schematic device structure can be found in Fig. 3.7. Similar to a top contact, bottom gate OFET, the source and the gate electrode are separated by the gate dielectric and the organic semiconductor material. However, the drain electrode does not align on the same level as the source electrode but overlaps it, only separated by a further organic semiconductor layer. A characteristic feature is that the width of the source electrode and the width of the gap w_{gap}, i.e. the distance between two neighboring parts of the source electrode can be rather large in comparison with the CIMT, introduced above. Thus, in order to prevent a direct current flow from the source to the drain contact, e.g. at a constant driving voltage, an insulating layer is deposited above the source. This is a common feature of all such devices which are called either VOFET or vertical organic thin film transistor (VOTFT) [117, 290–293]. The device concepts, VOTFT and CIMT have some similarities: For example, some VOTFTs do not have organic semiconductor between the source electrode and the gate dielectric, so that both layer layouts resemble each other. Nevertheless, the crucial difference is that the VOTFT performs better if the contact resistance is minimized whereas a CIMT needs a Schottky-barrier at the source contact to be able to modulate the injection resistance [117]. Despite the fact that the working mechanism is still under investigation, some first conclusions about the modulation of the current flow can be drawn. Since there is no need for contact resistance, a modulation of the charge transport instead of charge injection is likely which mainly means that the charge carrier concentration in the organic semiconductor layer is varied. Further, it is obvious that the source as well as the drain contact form a MOS capacitor together with the gate electrode, so that at a low driving voltage and a large gate potential, charge accumulation at the interface to the gate dielectric must be assumed. Then, it is imaginable that charges are injected at the source contact, flowing downwards into the channel region along the gate dielectric. Here, they will be laterally transported towards the region where the drain exclusively overlaps with the gate because the charge concentration in the channel is lower underneath the drain due to the lower voltage between drain and gate (cf. Fig. 3.7). However, there will be a transition region in the charge channel where the charge carrier concentration decreases from the level as realized underneath the source to the level which is present more distant from the source electrode. In this region, the local electric potential can be higher than that of the drain which leads to a net current flow towards the drain. This understanding of the working mechanism is further supported by the nearly bidirectional operation of such a device [117].

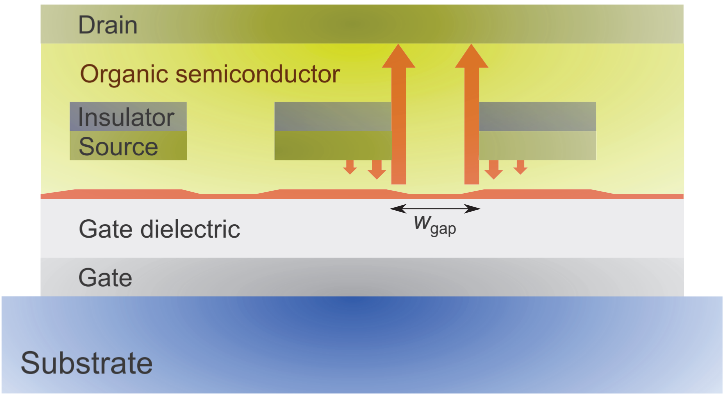

Figure 3.7: Schematic structure of a vertical organic thin film transistor. The arrows symbolize the current flow, whereas the red region is related to the charge accumulation at the gate dielectric and the thickness indicates the charge carrier concentration. The present understanding of the device assumes that charges are injected at the source, flowing downwards into the channel region where they are laterally transported and finally conducted to the drain.

Literature overview The device concept is also applied for inorganic electronics, realizing high-power switching transistors with large breakdown voltages and low on-state resistance [294,295]. These vertical insulated gate field-effect transistors are capable to drive more than 1 kA/cm^2 at a driving voltage of 10 V. For organic electronics, there is only a small number of publications considering this device concept [117, 290–293]. In 2004, Hirashima *et al.* used polysterene spheres to structure openings in a source electrode, having an insulating layer on top. The working mechanism remained unclear and so it is not fully clear whether this work reports a CIMT or a VOTFT. Although the transistor operated at 3 V, the current density of 25×10^{-3} mA/cm^2 remained rather low, but the proof of concept was successful. In 2006, Nakamura and coworkers presented pioneering results by integrating an OLED directly into the layer stack [291]. At a driving voltage of 10 V, they achieved current densities above 10 mA/cm^2 and luminance values of ca. 300 cd/m^2 which would be sufficient for display applications. Two years later, they were able to demonstrate a 16x16 pixel OLED display on plastic foil [292]. Interestingly, although the gap between two adjacent source electrodes w_{gap} was 100 µm, a homogeneous light emission in that region has been observed which points out that charges were able to flow at least 50 µm in lateral direction. Despite the promising results, these investigations have not been continued and no further work has been shown by this group. However, Kleemann *et al*. reanimated the device concept in 2013 and used photolithography on organic semiconductor layers in order to structure the source and the insulating layer on top in one process step [117]. Thus, both layers were perfectly aligned. At a driving voltage of 5 V, a current density about 50 mA/cm^2, and a large on/off ratio of ca. 10^6 were realized. They discussed the occurrence of contact resistance and argued that due to the short channel of the device further performance increase might be determined by the optimization of the charge injection at the source contact. In 2014, Keum *et al*. built a VOTFT with an integrated OLED underneath the drain electrode [293]. They investigated the light emission profile within the aperture of their metallic source network electrode, having gaps w_{gap} in size of 5,10, and 20 µm. It has been found that there is a localized intensity peak of the light emission near the edge of the source, decaying in both directions. The full width of half maximum of the distribution is estimated to be about 4 μm. As a consequence, the lateral current flow in this device seems to much smaller than observed by Nakamura [292]. Currently, it is unclear which device parameter exactly determines the lateral charge transport. In order to realize a short channel device, this length must be decreased to a minimum.

Advantages and disadvantages The idea of the VOTFT seems to be promising because there is no need for sub-μm structuring of the electrode or for any openings in the source electrode and nonetheless short channel devices are achieved. Other devices, like OLEDs, can be directly integrated or stacked on top. It is also a plus that this devices exhibit a high on/off ratio and a high current gain as known from OFETs. Although the channel length is expected to be much smaller than that of an OFET, the current density of such device does not clearly exceed such of standard lateral devices. One drawback may be that short channel devices are not anymore restricted by the charge transport in the channel but by contact resistance. As long as this is the case, a reduction in channel length does not necessarily lead to a strong increase in performance. For that reason, the working mechanism, especially, the charge flow and the charge carrier distribution, has to be understood in more detail. Then, this type of vertical organic transistor might develop to an interesting alternative to lateral-type OFETs with an automatic formation of a short channel.

3.2.5 Development of the scientific output

The progress in the field of vertical organic transistors can be visualized by the number of publications per year as shown in Fig. 3.8. As done in this section, each work is divided into one of four categories: VOT with or without structuring of the base electrode, CIMTs, and VOTFTs.[3] The corresponding references can be found in the literature overview of each device concept.

In order to decide whether a transistor is a vertical organic transistor, it has been to be proven how much the device function depends on inorganic parts and whether it is possible to exchange them without loosing the device functionality. Further, there must be a larger current flow perpendicular to the substrate surface. For example, vertical organic hybrid transistors have not been taken into account, because they use organic as well as inorganic materials as the semiconductors [296–303]. However, it is clear that the gate dielectric as well as the electrode often consist of inorganic materials. Other concepts, like step-edge OFETs have been excluded because they are considered to be a distinct topic and will be discussed separately.

Fig. 3.8 demonstrates that there is a rising interest in the field of vertical organic transistors. After the first publications appeared in 1994, it took some years until a larger scientific output has been generated. In 2004 and 2005, the work by Ma *et al.* as well as by Fujimoto *et al.* have triggered a wave of following investigations. Starting from the year 2007, at least 10 publications per year emerged and in 2013 as many as 18 papers can be found. Most articles deal with VOTs having a middle base electrode. Especially, those devices with an unstructured base can

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[3] The search includes use of 'Web of Science' and 'Google Scholar'. Typical keywords are 'vertical organic transistor', 'organic permeable base transistor', 'organic metal-base transistor', 'vertical organic field-effect transistor', 'organic static induction transistor', 'vertical organic triode'. Further, references and citing publications of highly relevant publications have been checked. For some authors, their scientific output is regularly searched. There is no certainty that all publications are found, but it can be assumed that a high percentage is listed as of this writing.

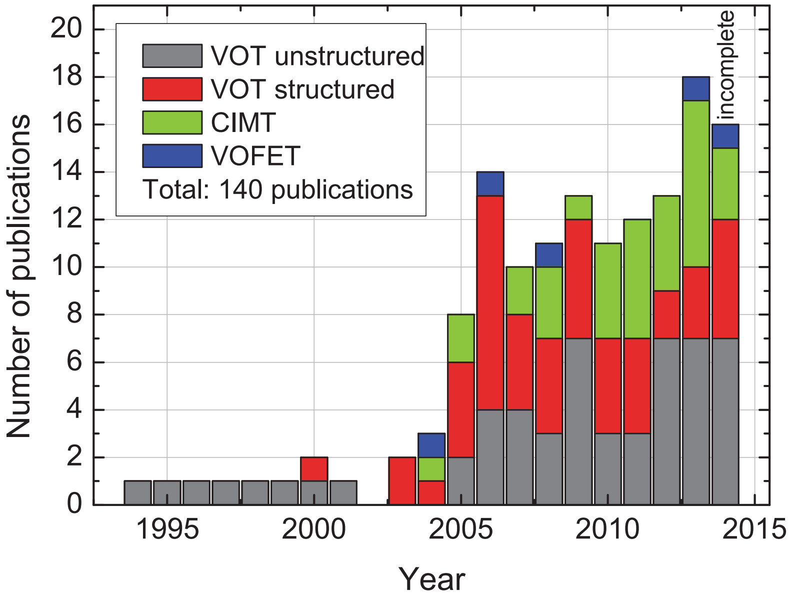

Figure 3.8: Number of publications per year for different vertical organic transistors.

be easily reproduced by other groups. Also, the CIMT enjoys a rising interest in the last years. However, most results have been reproduced by only one particular group. This is related to the fact that the structuring techniques for the source electrode require a specialized knowledge hampering the reproduction of the device. Although the VOTFT is one of the most promising device concepts because it has the potential to combine an OFET-like device behavior with a short channel achieved by low resolution structuring techniques, less studies have been performed on this topic. One can anticipate that there will be further progress on this topic.

In general, the trend points to a further growth of the output for the whole scientific field. Nevertheless, the number of techniques and concepts currently under investigation demonstrates that the ideal device structure has not been found, yet. It can be expected that it will be revealed in the next years whether vertical organic transistors can excel lateral TFTs devices or whether they will be outperformed by them due to improvements in lateral structuring, new materials and better reliability.

3.2.6 Competing technologies and approaches

Besides vertical organic transistors, there are other opportunities to either shrink down the channel length or to increase the charge carrier mobility of the semiconducting material without loosing the advantages associated with plastic electronic. Two of them will be discussed here.

Step-edge vertical channel organic field-effect transistors

Short channel OFETs can be realized by utilizing sharp step-edge structures. The corresponding transistors are called step-edge vertical channel organic field-effect transistors (SVC-OFETs). A

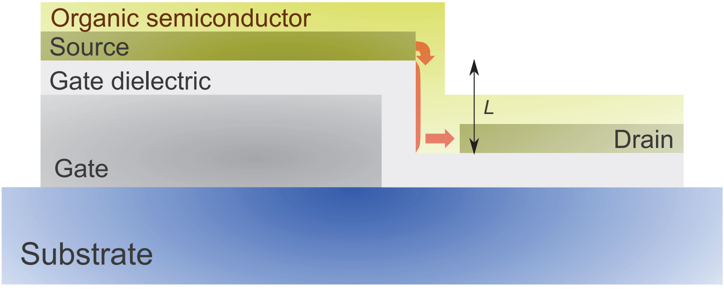

Figure 3.9: Schematic structure of a step-edge vertical channel organic field-effect transistors. A sharp step at the edge of the gate electrode with a height of a few 100 nm is utilized to deposited contact which are disconnected at this edge and thus can be used as source and drain. The channel length *L* of this device given by the accumulation of charge carriers at the gate dielectric will be in the range of the height of the step-edge structure.

schematic view onto the device layout is presented in Fig. 3.9. There are several ways to build them, but one popular method consists in using a sharp step-edge of an electrode which will be later used as the gate. The edge should be nearly perpendicularly aligned to the substrate and the height typically is in the range of 100 nm. After depositing the gate dielectric, metal is deposited under a certain angle onto the substrate, so that the resulting thin film is disconnected along the edge. As a consequence, two independent electrodes form which can be used subsequently as the source and the drain. Finally, the organic semiconductor is applied to the substrate. In the on-state of the device, a charge accumulation originates along the gate dielectric with a channel length *L* in the range of the thickness of the step height. Such devices have been demonstrated by several groups [304–309]. For example, Uno et al. have realized an SVC-OFET with a channel length of 500 nm and the molecule DNTT as organic semiconductor, having an effective current density of 12.6 A/cm^2 at a driving voltage of 5 V [306]. The transistor further exhibits an on/off ratio of 10^5 and a switch-on speed of 0.2 µs, corresponding to a transit frequency above 1 MHz. A drawback is that the step-edge feature has been achieved by etching of silicon, so that substrates like glass or plastic foils cannot be used. However, later this group was able to realize SVC-OFETs on bendable plastic substrate [306, 309]. Indeed, the effective current density decreased by nearly one order of magnitude, but at a driving voltage of 10 V, they achieved even slightly higher switching speed [309]. Despite the outstanding performance of the device, the estimated charge carrier mobility remains below 1 cm^2/Vs although the molecule DNTT is known to achieve higher mobility [110]. As a reason, limitations by contact resistance should be mentioned, being a general problem of devices with sub-µm channel length. Furthermore, the highest mobilities are often reached due to the formation of a herringbone pattern of the molecules on the gate dielectric [18]. In the case of a vertically aligned channel, this might be more difficult to achieve. Nevertheless, if such step-edge features can be realized on large scale with a good homogeneity, SVC-OFETs will become an interesting alternative to lateral OFETs as well as vertical organic transistors.

Oxide semiconductor TFTs

Often, remarkable achievements are related to new materials and their properties. Oxide semiconductors such as ZnO, SnO_2, indium-gallium-zinc-oxide (IGZO or GIZO), indium-zinc-oxide (IZO), zinc-tin-oxide (ZTO), indium-zinc-tin-oxide (IZTO), or indium-molybdenum-oxide (IMO) which can be used to build lateral oxide TFTs [310], have been received intensive attention in the past. A common feature of these materials is their good stability under ambient conditions which defines a significant advantage over most organic semiconductors. Furthermore, they can be structured by conventional photolithography, simplifying integration into existing industrial production processes. These materials can typically be fabricated by sputtering or pulsed laser deposition. In the last years, solution-processed oxide semiconductors have been widely investigated. Solely in 2013, more than 90 publications appeared on this topic which is nearly as much as the total scientific output for vertical organic transistors [311]. Solution processing allows for a cost-effective fabrication of the semiconductor layer [312]. For example, one possibility is to spin coat solutions with molecular precursors and subsequently anneal them to form the oxide semiconductor layer [313].

The large interest in oxide semiconductors arises from the fact that charge carrier mobilities over $10\,\mathrm{cm^2/Vs}$ can be achieved, making these materials competitive with poly-Si [110]. For example, Chasin *et al.* fabricated an IGZO diode still rectifying in the GHz regime and Münzenrieder *et al.* demonstrated an IGZO TFT with a transit frequency of 135 MHz [314, 315]. High charge carrier mobilities further allow for driving display pixels without the need for an aggressively downscaled channel length of the TFT. Thus, such oxide semiconductor transistors are considered to be part of future high-end displays with high resolution and high image refresh rate [310, 312]. The fact that the highest processing temperature can be below $250\,^\circ\mathrm{C}$ opens up the opportunity to fabricate on plastic foils. It has been demonstrated that such oxide TFTs still work if bent [312, 316]. Furthermore, they can be transparent, making them interesting for optoelectronic applications such as transparent displays [310]. Oxides also have the advantage that different materials are available, involving a material and processing platform to realize gate dielectrics, semiconductors, or electrodes, and the individual properties can be further tuned by the stoichiometry of the material [310].

However, drawbacks are that these outstanding properties often exclude each other. For example, low fabrication temperatures and solution processing also produce a lower charge carrier mobility, so that much effort is spent on improving the performance [313]. A further frequently discussed problem of oxide TFTs is the bias stress stability of the threshold voltage [312]. In contrast to that, contact resistance does not play a significant role which might be explained by the usage of techniques like plasma treatment or post process doping of the oxides, and proper choice of the contact material [312]. If further progress leads to an elimination of residual problems and the outstanding device performance achieved in various scientific works can be combined in a single device structure, oxide TFTs have the potential to become the dominant transistor technique for displays and plastic electronics in general.

3.3 VERTICAL ORGANIC TRIODES

VOTs with unstructured base electrode have been introduced in Sec. 3.2.1. The results presented in this work are based on this concept and will be discussed here in more detail. These devices are often referred to as Vertical Organic Triodes in analogy to vacuum tube triodes having the same abbreviation like a Vertical Organic Transistor: VOT. However, there is no difference between them. The designation "Triodes" comes from the greek word "tri hodos", meaning that there are three ways, and is principally applicable for every three-terminal device. In this section, the current flow in the device is shown, based on the device structure and a simplified energy diagram. However, the mechanism of charge transmission through the base will not be discussed as this will be part of the results in Chapter 5-7.

3.3.1 Stucture

Figure 3.10 visualizes the structure of a Vertical Organic Triode. The three electrodes emitter (E), base (B), and collector (C) are planar metal layers, stacked over each other, only separated by organic semiconducting layers. Emitter and collector have to ensure proper conductivity and their layer thickness is not of interest as long as the electrode resistance is low, so that typically more than 50 nm are used. The base electrode, however, has to be thin (ca. 10 - 20 nm) in order to allow charges to be transmitted, independent from the transmission process. Between the electrodes, the semiconductor layers are named according to the adjacent outer electrode: emitter layer or collector layer. Additional layers close to emitter or collector are optional and can be used to enhance the injection of charge carriers from the metal into the organic semiconductor. For example, this can be done by dopant molecules mixed into a layer of matrix molecules or a single dopant layers. From the sketch, the device is symmetric to the base electrode and the assignment of the electrodes as the emitter or the collector, a priori, is not possible. Thus, the bottom electrode could also be used as the emitter, and the top electrode as the collector. Only the middle electrode is unambiguously identified with the base. The direction of charge transmission has to be tested for every layer system, given by the materials used for the lower organic semiconductor, the base electrode, and the upper organic semiconductor. Moreover, the charge flow depends on the morphological and the energetic arrangement around the base electrode.

3.3.2 Electronic configuration

An independent electric potential V_i can be applied to each electrode, and the voltages between them are given by

$$V_\mathrm{ji} = V_\mathrm{j} - V_\mathrm{i} \tag{3.13}$$

where i,j equals to E, B, and C. For example, the driving voltage of the transistor is given by the potential drop V_CE between collector and emitter. The currents, flowing through the emitter (I_E), the collector (I_C), and the base (I_B) electrode can be measured externally. The technical current

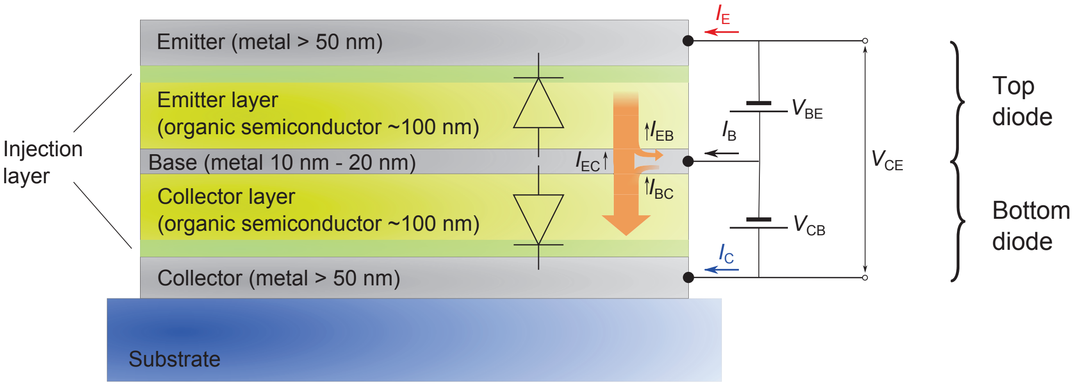

Figure 3.10: Structure of a Vertical Organic Triode, having a top and a bottom diode back-to-back. The main charge flow I_{EC}, indicated as an orange arrow, goes from emitter to collector. Leakage currents from emitter to base (I_{EB}) or from base to collector I_{BC} directly influence the transistor performance like current gain or on/off ratio, respectively. The electronic configuration shows the definition of the currents and voltages as they will be used for the description of the device.

direction, as used in this work, is given in Fig. 3.10. It is defined in a way that electrons flowing out of the device are associated with positive currents. The Kirchhoff's node law reads then

$$I_E + I_C + I_B = 0 \tag{3.14}$$

Nevertheless, the situation is different inside the device. Each current splits there into internal currents given by I_{ij} describing charge flow of electrons from the electrode i to the electrode j (i,j = E, B, and C). The set of equations

$$\begin{aligned} I_C - I_{EC} - I_{BC} &= 0 \quad (3.15)\\ I_E + I_{EC} + I_{EB} &= 0 \quad (3.16)\\ I_B + I_{BC} - I_{EB} &= 0 \quad (3.17)\end{aligned}$$

describes the relation between the external and the internal currents. Due to Eq. 3.14, there are three unknown internal currents but only two independent external ones, so that it is not possible to solve the equations unambiguously. As a consequence, the most interesting current, the transmission current I_T associated with I_{EC}, cannot be determined by the measurement.

3.3.3 Energetic alignment of the diodes

The base electrode forms a diode with either the top or the bottom electrode via the intermediate organic semiconductor, called top or bottom diode. These diodes are arranged back-to-back. They are connected by the base electrode, i.e. the interfaces between the base and the semiconductor layers are always rectifying whereas under ideal conditions the charge injection at the outer electrodes can be understood as Ohmic. This behavior is independent whether the VOT,

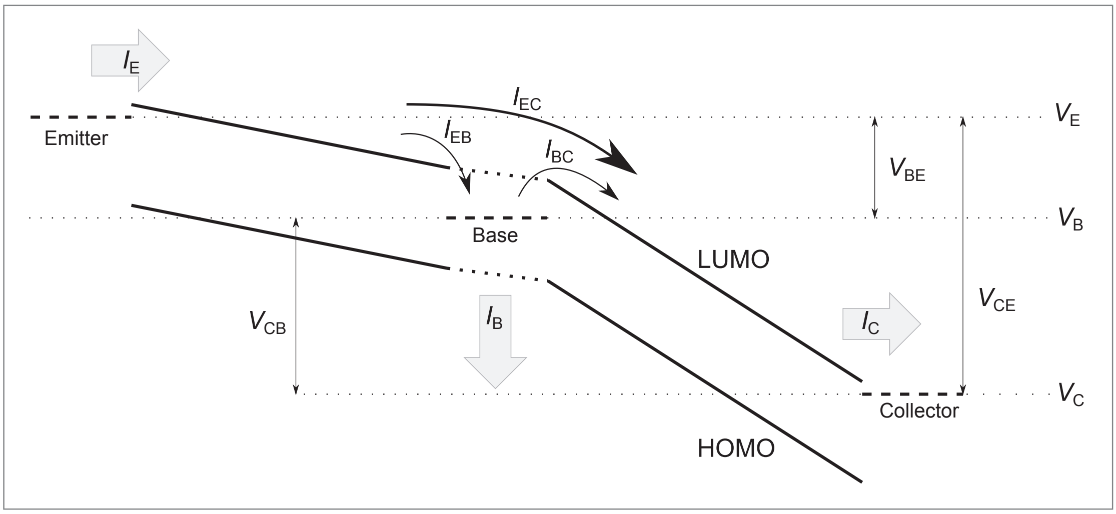

Figure 3.11: Schematic energy diagram of a Vertical Organic Triode. Arrows, associated with currents, indicate the motion direction of electrons.

being a unipolar device, is of n- or p-type. A more detailed understanding of the current flow can be obtained by considering the energy diagram of the device presented in Fig. 3.11. Here, a potential configuration of an n-type VOT is shown in which a substantial transmission current can be realized. The metallic electrodes are represented by their Fermi levels (dashed lines) shifted away from each other due to the externally applied voltage. If no voltage is applied, a common Fermi level across the entire device can be assumed. The organic semiconductor layers are represented by their charge transport levels for holes (HOMO) and electrons (LUMO. The respective black lines extend into the region of the base by dotted lines to symbolize a possible pinhole formation in this electrode. For clarity, no injection layers are inserted, but in order to indicate the two diodes, the electron injection barrier at the emitter and the collector contact are chosen to be smaller than between base contact to the two adjacent semiconducting layers.

Since the diodes are arranged back-to-back and both the voltages V_{BE} and V_{CB} are considered to be positive, the emitter diode (BE diode) is biased in forward and the collector diode (BC diode) in reverse direction. Thus, charges are injected at the emitter, flowing towards the base. A large part of the emitter current,

$$I_{\mathrm{EC}} = -\alpha I_{\mathrm{E}} \quad , \tag{3.18}$$

is transmitted with the transmission ratio α. After reaching the collector layer, the electrical field between collector and base conducts the charges to the collector.[4] The part of the emitter current which drops into the base electrode is

$$I_{\mathrm{EB}} = -(1-\alpha) I_{\mathrm{E}} \, . \tag{3.19}$$

It can be understood as loss (EB leakage current) since it has to be conducted away in order to keep the base potential unaffected and thus it is instrumental to realize the transmission current. Besides that, there is a BC leakage current I_{BC}, flowing from the base to the collector, realized by the applied electric field between both electrodes. However, since the collector diode is operated

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[4] The minus sign originates from the definition of the technical current direction.

in reverse direction, this current should be small due to the high electron injection barriers at the base contact, so that in the on-state of the device $I_{EC} \gg I_{BC}$ can be assumed. Finally, there might occur an EC leakage current, flowing from the emitter to the collector, characterized by its independence from the base-emitter voltage, but influenced by the driving voltage V_{CE} of the VOT (not shown in Fig. 3.11).

3.3.4 Current flow in the on and the off-state

In order to understand how the device switches the current flow off or on, an energy diagram of the off and of the on-state is presented in Fig. 3.12 for the same driving voltage V_{CE}. A low base potential realizes the off-state in which the base-emitter voltage is also low. The emitter does not inject current and thus current can neither be transmitted to the collector ($I_{EC} = 0$) nor drop in to the base ($I_{EB} = 0$). The main current flow is then determined by the BC leakage current, increasing by raising the collector-base voltage. There might also be an EC leakage current. However, this type of leakage current can easily be avoided by designing a device structure which avoids direct emitter and collector overlap. Its presence can be detected by a measurement with a constant driving voltage if a current plateau appears for switching the transistor off. Although the VOT is a unipolar device, the presence of minority charge carriers can not be excluded, e.g. holes in an n-type VOT. In the off-state, it is unlikely that they can be injected at the base contact due to the low base-emitter voltage, so that a larger collector-base voltage might lead to a relevant charge injection of holes as indicated in Fig. 3.12 a). There are two possibilities. The holes can either drop into the base, slightly increasing the BC leakage current, or be transmitted to the emitter. In both cases, the operation of the VOT is less disturbed as long as the BC leakage current realized by electrons remains higher.

For the on-state, the base-emitter voltage is increased by a high base potential, leading to a large current injected at the emitter. Nevertheless, there should still be a small voltage drop between collector and base in order to realize a transmission current with a high transmission factor [182]. Again, injection of holes at the collector can be neglected due to the low collector-base voltage, and by the fact that the collector current will be several orders of magnitude larger than the transmission current. In contrast to that, hole injection at the base into the direction of the emitter enhances I_{EB} as well as I_E, eventually reducing the transmission factor and the current gain. Especially, if one would like to reach a very high current gain above 10^4, similar to an OFET, this kind of hole leakage current can become more relevant.

The on/off ratio of the VOT

$$\text{On/off ratio} = \left. \frac{I_{C,\text{on}}}{I_{C,\text{off}}} \right|_{V_{CE}=\text{const.}} \tag{3.20}$$

is the ratio of current flow at the collector in the on and in the off-state. A high value in the range of several orders of magnitude is necessary to meaningfully use the transistor as a switch in an electronic circuit. There are two strategies to optimize this ratio: On the one hand, the charge injection at the base contact must be suppressed by either using material combinations forming a Schottky-barrier, or by an electrical passivation of the base. On the other hand, organic semiconductor materials with a high charge carrier mobility have to be used, and an Ohmic contact at the emitter is mandatory in order to enable the highest possible currents in the device. An

a) Off-state b) On-state

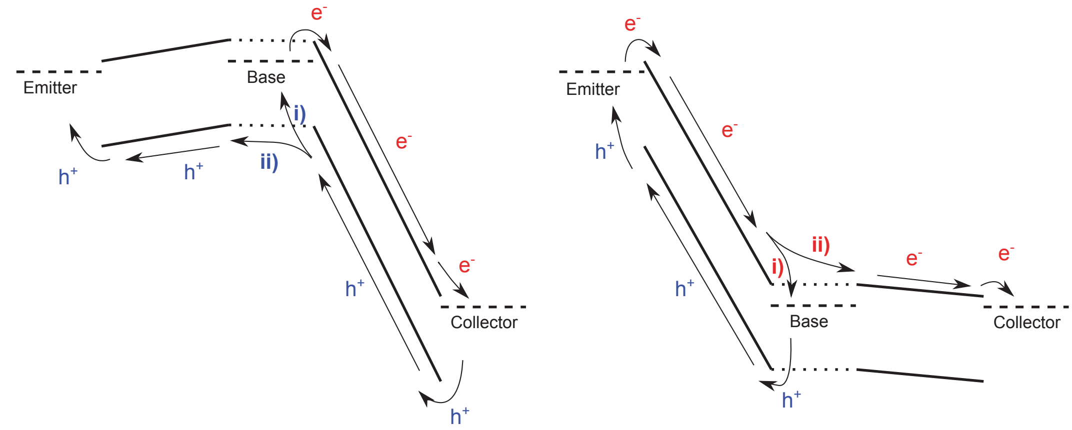

Figure 3.12: Schematic energy diagram of a) off-state and b) on-state. The VOT is a unipolar device and electrons (e^-) are majority charge carriers in this example. Holes (h^+) are minority charge carriers and are not necessary for device function. They rather lead to a parasitic current flow, disturbing the device performance.

optimization of the transmission process does not lead to a significant improvement of the on/off ratio since the transmission of a working device is already close to one.

3.3.5 Definition and extraction of parameters

Transmission and current gain Equation 3.22 defines the actual transmission of the VOT by comparing the transmission current with the injected current at the emitter. In reality however, the transmission current is unknown as a consequence of the base-to-collector leakage current I_{BC} and measuring the transmission by

$$\alpha_{\text{meas}} = -\frac{I_C}{I_E} \tag{3.21}$$

would lead to erroneous results which overestimate the transmission and the current gain since $I_C > I_T$, as the BC diode is driven in reverse direction. A correct determination of the actual transmission current as well as of the transmission factor is not possible as long as the current injected at the base into the collector layer is unknown. Principally, one can determine I_{BC} by measuring the collector diode with disconnected emitter, but it remains unclear whether this current flow is changed in the presence of transmission currents. However, if either the criterion $I_T \gg I_{BC}$ or $I_{BC} = 0$ at $V_{CB} = 0$ is fulfilled, one can assume that the collector current almost equals the transmission current, and the direct transmission is calculated by

$$\alpha = \left|\frac{I_T}{I_E}\right| \sim \left|\frac{I_C}{I_E}\right| = \alpha_{\text{meas}} \quad . \tag{3.22}$$

This situation represents an ideally working VOT. Then, the measured transmission α_{meas} coincides with the actual transmission α which is present as an intrinsic property of the base elec-

Transmission α	0.1	0.5	0.9	0.99	0.999	0.9999
Current gain β	0.11	1	9	99	999	9999

Table 3.1: Comparison of values for transmission and current gain

trode. Furthermore, the direct current gain

$$\beta = \frac{I_{\mathrm{EC}}}{I_{\mathrm{EB}}} = \frac{I_{\mathrm{C}}}{I_{\mathrm{B}}} = \beta_{\mathrm{meas}} \tag{3.23}$$

can be easily determined by the externally measurable currents, too. One can further show that the direct transmission factor and the direct current gain are related to each other by

$$\beta = \frac{-\alpha I_{\mathrm{E}}}{-(1-\alpha) I_{\mathrm{E}}} = \frac{\alpha}{1-\alpha} \tag{3.24}$$

which means that the physical process of charge transmission through the base is directly linked to the technical property of current amplification necessary to describe the transistor action in an electrical circuit. Table 3.1 presents values of the current gain achieved for different transmission factors. To reach a direct current gain of more than one, the transmission current must be higher than 50% of the emitter current. A high current gain is only achieved if the transmission is close to one. For example, a bipolar junction transistor has a current gain of about 100 which equals a transmission of 99%. Field-effect transistors work in DC mode without any gate current and have a large current gain typically greater than 10^4, only limited by residual leakage currents, so that more than 99.99% of the charges injected at the source contact reach the drain contact.

Experimental test structures of VOTs, however, often have a low on/off ratio, or the transmission might be investigated at lower emitter currents. In both cases, the transmission current is still higher than the BC leakage current, but the criterion $I_{\mathrm{T}} \gg I_{\mathrm{BC}}$ might not be valid. Then, there is the need for evaluation strategies which consider deviations from ideality. This can be done by determining an estimate for the quality of the measured current gain $\beta_{\mathrm{meas}} = I_{\mathrm{C}}/I_{\mathrm{B}}$. Such a relation is derived in the Appendix (cf. Sec. A.1). One can show that the ratio $r = I_{\mathrm{EC}}/I_{\mathrm{BC}}$ between the transmission current and the BC leakage current has to fulfill the relationship

$$r \geq \left(1 + \frac{1+\eta}{1/\alpha - 1}\right)\frac{1}{\eta} \tag{3.25}$$

in order to achieve an agreement to the current gain related to the actual transmission α within a maximum relative deviation of $\eta = \beta_{\mathrm{meas}}/\beta - 1$. For example, a current gain of 100, corresponding to a transmission of ca. 99%, can be specified within a maximum deviation of $\eta = 10\%$ if the BC leakage current is at least 1110 times lower than the transmission current.

Another evaluation strategy is to use the differential transmission $\alpha_{\mathrm{diff}} = -\partial I_{\mathrm{T}}/\partial I_{\mathrm{E}}$. If the transmission current is proportional to the emitter current, meaning that $\alpha(I_{\mathrm{E}}) = \text{const.}$, differential and direct transmission are equal. In the case of a transmission decreasing with the increase of the absolute value of the emitter current, as typically observed for VOTs, the observed transmission value is below the direct transmission [182]. As a consequence, the differential transmission

$$\alpha_{\mathrm{diff}} = -\frac{\partial I_{\mathrm{T}}}{\partial I_{\mathrm{E}}} \leq -\frac{I_{\mathrm{T}}}{I_{\mathrm{E}}} = \alpha \tag{3.26}$$

represents a lower boundary of the direct transmission. This further implies that calculating the differential transmission automatically leads to an estimation of the direct transmission. Therefore, the differential measured transmission, being the collector current differentiated with respect to the emitter current,

$$\alpha_{\text{meas,diff}} = -\frac{\partial I_C}{\partial I_{\text{E}}} = -\frac{\partial (I_{\text{T}} + I_{\text{BC}})}{\partial I_{\text{E}}} < -\frac{\partial I_{\text{T}}}{\partial I_{\text{E}}} = \alpha_{\text{diff}} \leq \alpha \quad , \tag{3.27}$$

has the property to be always smaller than the differential transmission and the direct transmission. This is the case because the base-collector voltage increases monotonically with the emitter current, so that the relation $\partial I_{\text{BC}}/\partial I_{\text{E}} > 0$ can be applied. Thus, the calculated value is a good estimate for the minimal transmission of a VOT which can certainly be realized for a certain potential configuration.

Voltage gain and feedback The voltage gain of a transistor is defined by

$$\beta_{\text{V}} = -\frac{\partial V_{\text{CE}}}{\partial V_{\text{BE}}}|_{I_{\text{C}}=\text{const.}} = \frac{g_{\text{m}}}{g_{\text{d}}} \tag{3.28}$$

and is related to the transconductance

$$g_m = \left.\frac{\partial I_{\text{C}}}{\partial V_{\text{BE}}}\right|_{V_{\text{CE}=\text{const.}}} \tag{3.29}$$

and the output conductance

$$g_d = \left.\frac{\partial I_{\text{C}}}{\partial V_{\text{CE}}}\right|_{V_{\text{BE}=\text{const.}}} \tag{3.30}$$

being the inverse output impedance [317]. Thus, a current saturation in the output characteristics is necessary in order to reach a high voltage gain. The transconductance, however, should be large which can be realized by a steep increase of the collector current with respect to the base-emitter voltage as well as by a large current output in general.

Interestingly, the feedback of a transistor is directly related to the voltage gain, being the inverse of it. This parameter

$$D = -\left.\frac{\partial V_{\text{BE}}}{\partial V_{\text{CE}}}\right|_{I_{\text{C}}=\text{const.}} \tag{3.31}$$

describes the coupling between the emitter and collector, i.e. how the electrical field in the collector diode can punch-through the base, e.g. by openings, and influence the electric potential at the emitter contact. Sometimes, the feedback is also defined as

$$S = -\left.\frac{\partial V_{\text{BE}}}{\partial V_{\text{BC}}}\right|_{I_{\text{C}}=\text{const.}} \tag{3.32}$$

being the voltage feedback with the difference that the collector-base voltage is used instead of the driving voltage in the denominator [199, 301]. The parameter S can take values between 0 for a full electric screening as expected for a hot-electron transistor and 1 for no screening by the base electrode as realized by a permeable base transistor.

The relation between the feedback, the transconductance, and the output impedance is also often denoted by the equation

$$g_\mathrm{m} * D / g_\mathrm{d} = \beta_\mathrm{V} * D = 1 \tag{3.33}$$

and has been first applied to vacuum tube triodes.[5] It demonstrates once more that for achieving a high voltage gain as well as a pronounced current saturation in the output characteristics, a low feedback is necessary.

Small signal amplification Time dependent signals lead to a displacement current i_B at the base due to charging and discharging of the device capacitances [110].[6] Figure 3.13a) shows a schematic diagram for the currents of a VOT at various frequencies. At low frequencies, the displacement currents at the base are much lower than the normal base-to-emitter leakage current and the DC current gain β_I is obtained. However, at higher frequencies, the base displacement current rises proportionally to the frequency. Since the amplitude of the collector current i_C is assumed to be unaffected, the current gain decreases accordingly. When both base and collector current are equal, the unity-gain is reached, determining the transit frequency f_T which can be seen as the highest frequency where a transistor is able to work as an actively amplifying device. One can now compare with an OFET where the currents for the gate and the drain are denoted as i_G and i_D, respectively. It is assumed that the VOT and the OFET have the same current amplitude of the output signal as well as the same transit frequency. Due to the much higher DC current gain, the gate current of an OFET is given by displacement currents only, even at lowest frequencies. However, at frequencies higher than the transit frequency divided by the current gain of the VOT, both devices behave similarly. As a consequence, the DC current gain does not play a role for applications where small signals are amplified at high frequencies. Then, the current gain is described as

$$\beta_\mathrm{I} = \frac{|i_\mathrm{C}|}{|i_\mathrm{B}|} = \frac{g_\mathrm{m}}{2\pi f C_\mathrm{B}} \tag{3.34}$$

with C_B a device specific capacitance of the base. Whereas for OFETs the corresponding gate capacitance C_G can be deduced from the device geometry, an evaluation for VOTs has not been performed yet [110].

The situation is similar for the voltage gain β_V as presented in Fig. 3.13b), except for the fact that VOTs and OFETs do not qualitatively differ at low frequencies. Both devices have a constant voltage gain at the beginning which decreases when reaching the cutoff frequency f_C defined as the drop of the current gain by 3 dB, corresponding to a factor of $1/\sqrt{2}$. Then, the voltage gain falls inversely proportional to the frequency and reaches a unity-gain at $\beta_\mathrm{V} f_\mathrm{C}$ which is also called the gain-bandwidth product of an amplifier. The voltage gain is important for logic circuits in order to preserve the voltage potentials of the logic on- and off-state [317, supplemental material]. For that reason, the cutoff frequency has more relevance for practical applications since nearly the maximum voltage gain is still available.

By comparison of current gain and voltage gain, one can show that the transit frequency of the current gain is higher than the frequency where the voltage gain equals one [317, supplemental

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[5] This formula has been first written down by Hendrik van der Bijl in 1920 [2]. However, often this formula is associated with the "Barkhausensche Röhrenformel", named after the German physicist Heinrich Georg Barkhausen.

[6] Time dependent currents are indicated by small letters.

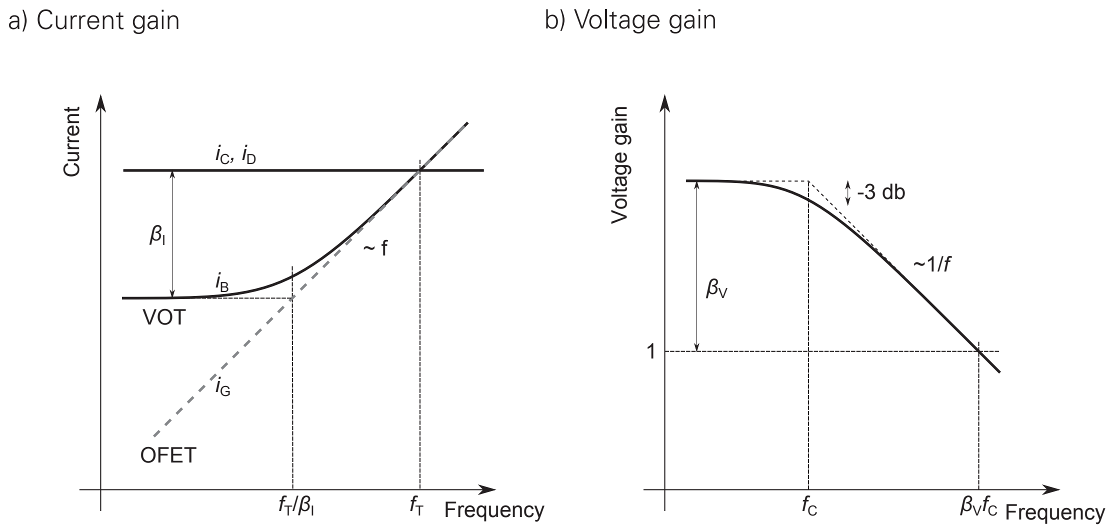

Figure 3.13: Diagrams, showing the frequency-dependent behavior for a) the current gain and b) the voltage gain. Please note that all scales are logarithmic.

material]. Thus, determination of the frequency dependence of the voltage gain, e.g. with a ring oscillator or an inverter circuit, can be used to estimate a lower limit of the transit frequency. It should be further mentioned that the voltage gain might be affected by a residual resistance of the base electrode R_B, enhancing the RC time constant to

$$\tau = R_B C_B = \frac{1}{2\pi f_C} \tag{3.35}$$

and thus decreasing the cutoff frequency. In contrast to that, the current gain remains unaffected because it does not matter which base-emitter voltage is necessary to realize a certain base current.

4 EXPERIMENTAL

This chapter introduces the processing and measuring techniques used in this work. The main focus is directed on the fabrication of vertical organic triodes by thermal vapor deposition. Special attention is given to the mask setup. Finally, the properties and characteristics of the materials are summarized.

4.1 GENERAL PROCESSING

4.1.1 Thermal vapor deposition

The deposition of the functional layer is done by thermal vapor deposition in high vacuum. Figure 4.1 schematically demonstrates the operating principle. A crucible evaporates material in upward direction, allowing to deposit only material sticking to the substrate. The thin films are structured by a shadow mask located near the substrate, explained in detail in the next section. A quartz crystal microbalance (QCM) monitors the material flow by changing its resonance frequency upon mass take-up. Thus, the thin film thickness can be determined with an accuracy of less than 1 Å. Prerequisite is a calibration of the QCM prior the layer deposition with a reference QCM at exactly the sample position, accounting for the different deposition rates at different positions in the chamber. The temperature of the crucible, used as a technical parameter to identify the operation range, is measured by a thermocouple of type K. However, the value does not necessarily correspond to the temperature of the material in the crucible, but will be in relation to it. The material flow can be controlled by shutters either in front of the crucible or the sample, e.g. allowing the deposition rate to be set before thin film processing starts. All deposition steps are made in a high vacuum chamber with a base pressure below 10^{-7} mbar, realized by a turbo pump with a prefixed forevacuum pump. There are several reasons for the need of vacuum conditions. Most of the organic semiconductors or dopant materials are not air-stable, so that they would degrade before the sample has been finished. Residual gas molecules could interfere with the material flow and also influence the thin film formation. Beyond that, the tungsten filaments used

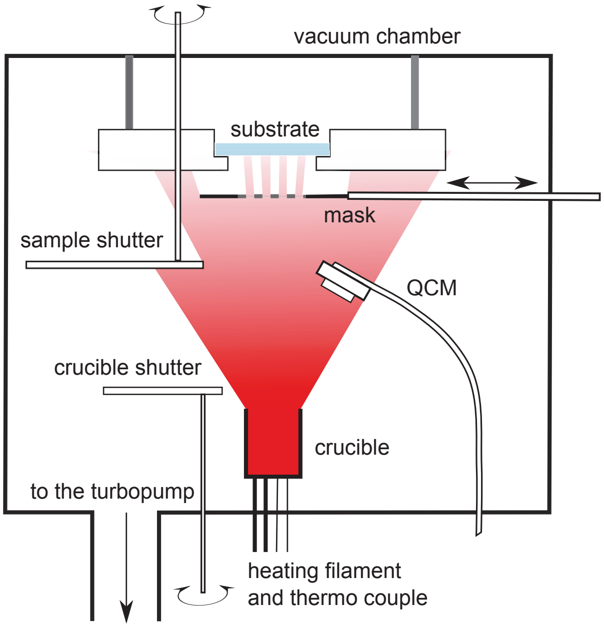

Figure 4.1: Schematic setup for thermal vapor deposition in vacuum. A heated crucible evaporates material in upward direction. A quartz crystal microbalance (QCM) measures the deposited thin film thickness, previously calibrated to the reference position of the sample. With the help of shadow masks, layers are structured. Shutters are used to control the material flow next to the sample or the crucible. A turbopump with a prefixed forevacuum pump realizes high vacuum conditions.

to heat the crucible would quickly oxidize and be destroyed. In each vacuum chamber, several materials are available, enabling co-evaporation of at least two materials. The temperature of each crucible can be controlled independently to control the material flow measured by a number of QCMs which are located in a way that they are only able to detect one crucible. Otherwise, the effect of crosstalk between the crucibles and the QCMs would prevent a correct determination of the materials mixing ratio. Thus, co-evaporation is a straightforward method for the fabrication of doped molecular layers.

4.1.2 Processing tools

There are two tools available for sample processing with thermal vapor deposition. A first setup is a multi vacuum chamber system from Bestec GmbH (Germany). It consists of a handler chamber from which the sample can be transferred to several other chambers without breaking the vacuum. In each chamber other materials can be processed. They are grouped according to their purpose, e.g. metals are in a single common chamber as well as intrinsic materials. Samples are transferred into the vacuum via a venting chamber which connects a glove box with nitrogen atmosphere to the handler chamber. Prior to transfer into the vacuum chamber, cleaned substrates are mounted onto a sample holder in a flow box before they are loaded into the glove box by an antechamber. This processing tool is used to fabricate samples for investigations with photoelectron spectroscopy, scanning electron microscopy, transmission electron microscopy, atomic force microscopy, and X-ray reflection/diffraction methods. The size of the glass substrates is 2.5 cm x 2.5 cm.

A second setup is a single evaporation chamber with the capability of sample variation on a single substrate, purchased from Kurt J. Lesker Company (USA). Glass substrates with a size of 15 cm x 15 cm can be processed, allowing to cut them afterwards into 6 x 6 2.5 cm x 2.5 cm large samples. In order to ensure a high uniformity of the layer thickness, the substrate rotates while evaporation takes place. As a consequence, differences in the distance between each sample to the current crucible get better equalized. An adjustable sample shutter, rotating with the substrate, allows for the control of material deposition onto specified rows or columns of samples on the substrate. With this technique, a specific layer of the device stack can easily be varied in thickness or skipped for some samples. The main advantage is that except for the varied layer, all samples have nearly identical layers, so that a comparison of the devices processed in a single run eliminates uncontrolled variations between successive runs. The materials to be evaporated are available in one chamber. There are four metal sources arranged close to the rotation center of the substrate and eleven crucibles for the evaporation of organic molecules located close to the wall of the circular chamber. Similar to the first setup, there exists a glove box and a venting chambers allowing to transfer the substrate into the vacuum. The processing is done by experienced operators who primarily work with this machine.

4.1.3 Processing information

Substrates Two different glass substrates are used. All devices except for OLEDs are produced on glass substrates (Borofloat 33, Schott AG[1]) (purchased from PRINZ OPTICS GmbH, Germany). The substrate used for processing of OLEDs is coated with predefined electrodes of indium-tin-oxide (ITO) a transparent conductor, purchased from Thin Film Devices Inc. (USA). In the region of the active area, the electrodes have a width of 2.54 mm. The 90 nm thick ITO has a sheet resistance of approx. 30 Ω/sq. and a transparency in the visible range of about 85 %. Both types of substrates have a thickness of around 1.1 mm and the heat conductivity is ca. 1.2 W/m/K.

Substrate cleaning Prior to processing, all substrates are cleaned with a defined procedure. The first step is an ultrasonic bath of the organic solvent N-Methyl-2-pyrrolidone (NMP) for 20 min, followed by rinsing for 5 min in deionized water. An ultrasonic bath is subsequently performed in deionized water and in ethanol, each step for 10 min. A spin rinser is used to dry the substrate (15 min) and finally an ultraviolet ozone cleaning system (UVOCS) removes last residuals for 10 min. Afterwards the substrate is loaded into the glovebox.

Device encapsulation Because of the missing air-stability of the used components, devices are encapsulated. This is done in nitrogen atmosphere, having less than 1 ppm of O_2 and H_20, within a glove box (purchased from M. BRAUN Inertgas-Systeme GmbH, Germany). The geometry of

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[1] product sheet: http://www.schott.com/borofloat

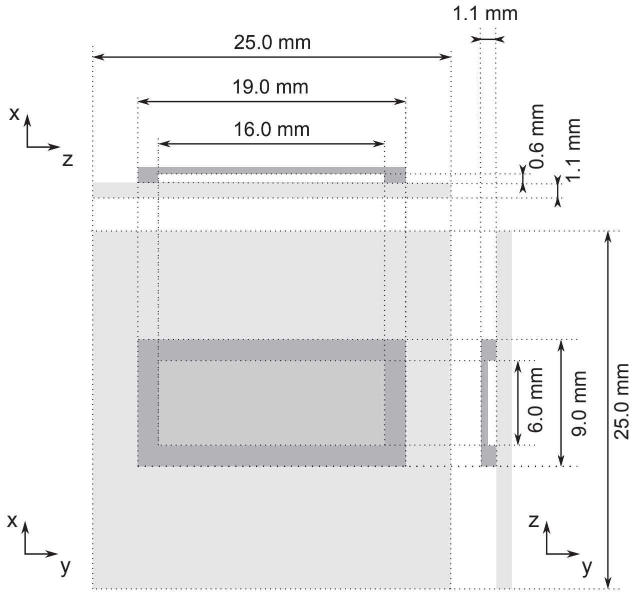

Figure 4.2: Geometry of the glass substrate and the encapsulation for a single 2.5 cm x 2.5 cm large sample.

the encapsulation glass is visualized in Fig 4.3. It is 1.1 mm thick and in the region of the active area, a 0.6 mm deep indentation ensures that the device is not touched by the encapsulation glass lid. An epoxy glue is employed to guarantee proper sealing and fixing of the encapsulation glass to the substrate. The glue is finally cured by exposure to UV light, protecting sensitive parts by a UV-opaque mask.

Annealing The annealing is done on a hot plate in a nitrogen filled glovebox ensuring no further exposure to oxygen. A Stuart Hot plate (purchased from Bibby Scientific Limited, United Kingdom) has a size of 16 cm x 16 cm, allowing to include all samples of a processing run in the same annealing step. A thick aluminum block ensures a good temperature uniformity. The temperature variation across the plate is better than 1 K at 150 °C. The annealing procedure starts with placing the samples on the hot plate at room temperature. Then, the temperature is set to 150 °C and after a time of 2 h, samples are removed from the plate without previous cool down. Subsequently, they are unloaded from the glovebox.

4.2 MASK SETUP

The general concept to fabricate electronic devices is based on the overlap of planar electrodes, evaporated through different shadow masks. The overlapping region defines the active area of the device. Functional layers are evaporated over a wider area and separate the electrodes, determining the characteristic device behavior. Typically, these electrodes are configured perpendicular to each other so that a certain parallel displacement of the mask or the substrate in the mask holder does not change the size of the overlapping area between the two electrodes. For electrical measurement, electrodes are contacted in an area where they do not overlap with organic layers nor

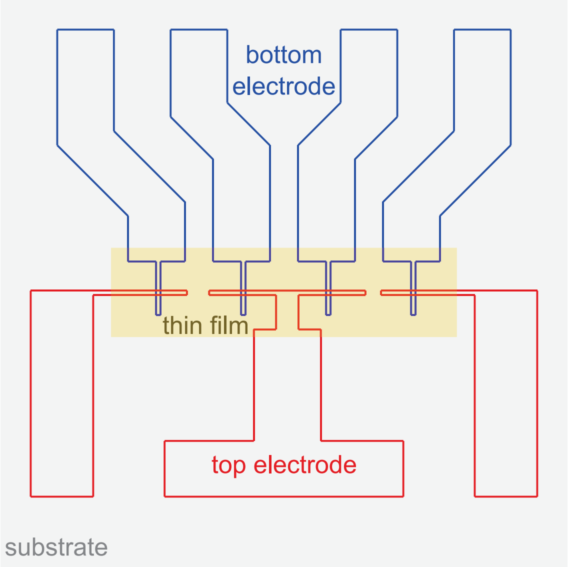

Figure 4.3: Mask setup for a two-terminal device. By the overlap of the top and the bottom electrode, four devices with a designated active area of approx. 200 µm x 200 µm can be realized.

each other. Such a setup is called crossbar architecture and can be efficiently used in combination with 'sandwich'-type layer configurations, such as OLEDs, OSCs, or VOTs. Three different sets of masks setups are used in this work applied in the previously introduced single evaporation chamber.

Two-terminal devices Devices with two-terminals are realized by the mask setup visualized in Fig. 4.3. On each sample, four independent devices are created, each with an active area of 200 µm x 200 µm. However, evaporated electrodes are broader than designated by the mask due to geometrical aspects of the evaporation process. Imaging by an optical microscope reveals an active area of approx. 250 µm x 250 µm which has been used to calculate the current density for this setup [318]. This setup is used for n-doped/intrinsic/n-doped C_{60} devices discussed in Sec. 9.

For processing of OLEDs, the setup is slightly different. The ITO electrodes are prestructured on each sample with a width of 2.54 mm, in a similar configuration as used for the bottom electrode in Fig. 4.3. The top electrode is processed by evaporation of a metal, realizing a continuous electrode perpendicular to the ITO electrodes with a width of 2.54 mm, so that an active area of 6.45 cm^2 originates. The layout is similar to the top electrode in Fig. 4.4, allowing to contact it from two sides.

Large active area vertical organic triodes Most experiments on vertical organic triodes are carried out with a structure having a larger active area of approx. 4 mm^2. The mask layout can be seen in Fig. 4.4. Four independent devices are created per sample by the overlap of all three electrodes. The bottom (blue) and the middle electrode (black) have four single electrodes whereas the top electrode (red) connects all devices. In contrast to a two-terminal device, a possible mask misalignment inhibits a perfect alignment of all three electrodes in the same area.

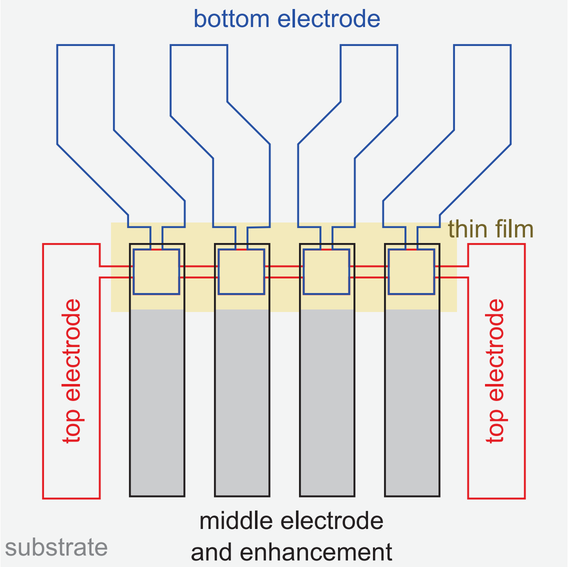

Figure 4.4: Mask setup for a large vertical organic triode. Four devices with a designated active area of approx. 2 mm x 2 mm can be realized.

The typical misalignment for the setup used in this work leads to an electrode displacement on the substrate of approx. 200 µm. In order to circumvent an exclusive overlap of top and bottom electrodes, used as emitter and collector, the middle electrode (base) is planned to be somewhat larger, so that even with an unavoidable misalignment, devices do not show an enhanced emitter-to-collector leakage current. As a consequence, there originate regions with exclusive overlap of an outer electrode with the middle electrode. Even at the best possible alignment of the electrodes, only 95% of the overlap of the top and middle electrode contribute to the active area given by the mask design. E.g. a typical misalignment reduces this ratio to approx. 85%, measured by optical imaging. Besides that, the electrode layout takes care for an enhancement in thickness of the middle electrode to regions outside the active area by a separate mask. This is necessary due to the fact that the base electrode is relatively thin compared to the other electrodes, and thus it incorporates a higher resistance which might also be affected by the encapsulation glue. Further masks for this electrode setup are available to define the active area by laterally structured insulating layers. In Sec. 8.4, they are introduced together with the related experimental results.

Small active area vertical organic triodes The mask set for vertical organic triodes with a small active area has to address the problem of misalignment in depth. An electrode displacement of ca. 200 µm is a serious challenge if the desired active area shall be 200 µm x 200 µm. For that reason, structuring of the active area with insulating layers is required. Figure 4.5 shows the corresponding mask setup. The electrode configuration to contact each device outside the encapsulation glass is similar to the design mentioned previously, so that here the concentration lies on the active area of one device. The misalignment is considered on the one hand by larger widths of the electrodes of 600 µm, exceeding the desired active area of 200 µm x 200 µm. This ensures that even for a certain electrode displacement, the overlapping regions remains sufficiently large. On the other hand, insulating layers are embedded between the electrodes used as emitter and base to restrict the charge flow to a specific area. Although it is not known where this area

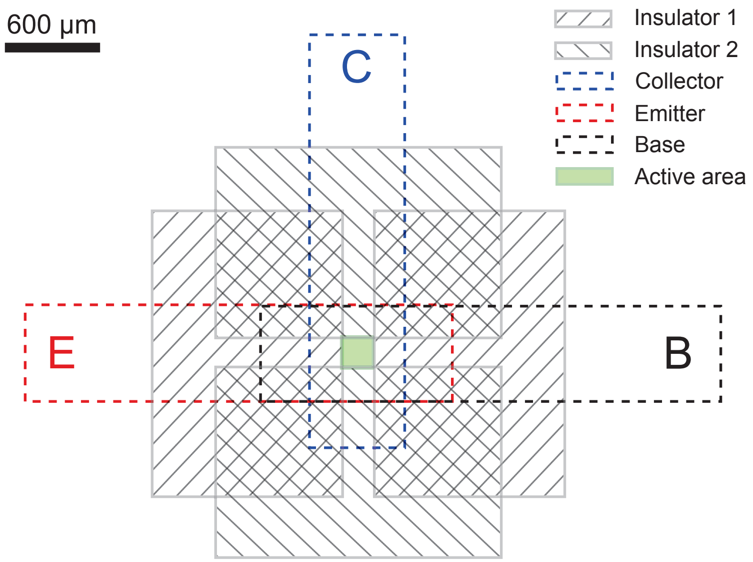

Figure 4.5: Layer setup for high-frequency triodes. Insulating layers are used to realize the active area of 200 µm x 200 µm. For each layer 'Insulator 1' and 'Insulator 2', a separate mask is used. The electrodes for collector, emitter, and base have a width of 600 µm. Please note that the insulated layer are deposited within the shaded areas.

creates in the overlap region of the electrodes, most importantly, its size remains unchanged. A single mask is not capable to realize a free but framed region laterally in the insulating layer because this would require a mask with a freestanding part corresponding to this position. For that purpose, two masks are applied with a strip of 200 µm width, positioned horizontally or vertically above the overlapping region of the electrodes. For each mask, insulating layers are deposited above and underneath or to the left and to the right of the strip. Thus, a central region remains free from the insulating material which is then considered to be the structured active area. Similar to the previous mask setup, the 600 µm wide top electrode connects again all four devices and the base electrode can be enhanced in thickness outside the active area by an additional mask.

4.3 MEASUREMENT SETUPS AND TOOLS

4.3.1 Current-voltage measurements

For electrical measurements of continuous currents, source-measuring units (SMU) are employed. These tools are able to work in four quadrant operation, meaning that they can act as a current source or sink independently from applying negative or positive voltages. This allows to operate them as current or voltage source, combined with measuring voltage or current. For example, they can be used as voltmeter or ammeter if current or voltage is set to zero, respectively.

Parameter Analyzer Keithley SCS-4200 Transistor characteristics are measured with a parameter analyzer Keithley SCS-4200. The instrument is equipped with three medium power SMUs 4200-SMU and one high power unit 4210-SMU. Each SMU is connected to one transistor electrode and can be configured independently from each other. Nevertheless, one SMU will realize a common potential, e.g. ground and thus determines the measurement configuration such a common-emitter or common-base connection. A second SMU keeps a certain parameter constant at which the third SMU makes a voltage sweep. The accuracy and the resolution of the parameter analyzer is well below the requirements. Independently from sourcing or measuring mode, the accuracy is better than $\pm 0.02\,\%$ of the measured value for voltages and $\pm 0.06\,\%$ for the current. The resolution of the voltage is at least 5 µV and the current can be measured down to 100 fA. However, cabling and contacting the sample reduces the current resolution to be no better than 10 pA in an open circuit but still low enough for the experiments performed in this work. To achieve the resolution specified above, the right measurement range has to be chosen. Therefore, the currents are measured with auto range and voltage with best fixed option. The measuring speed is set to normal.

Source-measuring unit Keithley 2400 For measurements of two-terminal devices like a C_{60} crossbar device with a layer sequence consisting of n-doped/intrinsic/n-doped or OLEDs, a SMU Keithley 2400 is used. It is a single unit, controlled over the GPIB interface by a home-built measuring software. The main difference to the SMUs of the parameter analyzer is a lower resolution by default in the current range of 10 pA. Other specifications are similar. It also allows to measure in 4-wire mode. Two additional sense terminals measure a voltage drop between two specific points in the circuit through which a current flow is generated by the source terminals of the SMU.

4.3.2 Frequency-dependent measurements

Frequency-dependent transistor measurements are performed in order to investigate their switching speed. A Hewlett Packard oscilloscope Infiniium 54815A traces the incoming and out coming signal as well as the power supply level. In order to realize a small signal sine wave, an Agilent

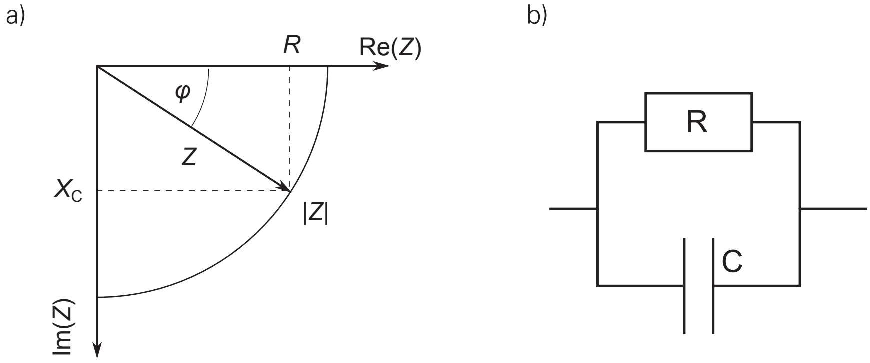

Figure 4.6: a) Schematic diagram of the complex impedance. b) Equivalent circuit to determine the total capacitance.

33220A (20 MHz function/arbitrary waveform generator) is used. If pulses have to be applied, a Hewlett Packard 8114A (100V/2A pulse generator) is taken. Investigated samples have an active area of ca. $4\,\mathrm{mm}^2$.

To reveal proper switching at high frequencies, further tests are made with a Parameter Analyzer Keithley SCS-4200 equipped with an ultra-fast I-V module 4225-PMU.[2] Two Keithley 4225-RPM (remote amplifier/switch) amplify the signals. This setup allows to simultaneously measure the current and the voltage signal of the base and the collector and thus enables an estimation of the transit frequency. Investigated samples have a structured active area of ca. $0.04\,\mathrm{mm}^2$.

4.3.3 Impedance Spectroscopy

For impedance spectroscopy, a 4284A precision LCR meter from Hewlett Packard (USA) is used. The method is based on the frequency-dependent response on a small signal superimposed by a constant offset for which the sample is investigated. For example, a voltage signal given by

$$v(t) = v_0 + v_{\mathrm{max}} * \sin(\omega t) \tag{4.1}$$

where v_0 is a constant offset, v_{max} a small signal amplitude, and ω the angular frequency ($2\pi f$), leads to a time dependent current flow

$$i(t) = i_0 + i_{\mathrm{max}} * \sin(\omega t + \phi) \tag{4.2}$$

in the device, where i_0 and i_{max} are the respective magnitudes for the current. The angle ϕ is related to the phase shift of the current with respect to the voltage signal, induced either by capacitances or inductivities in the device. The ratio between the amplitude of the voltage and the current signal determines the absolute impedance (modulus)

$$|Z| = \frac{v_{\mathrm{max}}}{i_{\mathrm{max}}} \tag{4.3}$$

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[2] The equipment has been kindly provided by NaMLab gGmbH (Dresden, Germany).

of the device. The Ohmic resistance R and the capacitive resistance X_C are the real and the imaginary part of the impedance Z, calculated by

$$R = |Z| \cos\phi \quad , \quad X_\mathrm{C} = |Z| \sin\phi \,. \tag{4.4}$$

The capacitance C is calculated, assuming a single RC element, by

$$C = \frac{-X_\mathrm{C}}{\omega |Z|^2} \,. \tag{4.5}$$

Thus, the given capacitance represents the whole device at a certain applied voltage v_0 [319]. Finally, the sandwich geometry allows for understanding the device as a plate capacitor, so that capacitances can be associated to layer thicknesses d by

$$C = \epsilon \epsilon_0 \frac{A}{d} \tag{4.6}$$

where A is the active area. ϵ and ϵ_0 are the relative and the vacuum permittivity, respectively.

4.3.4 Ultraviolet and X-ray Photoelectron Spectroscopy

Photoelectron spectroscopy is used in this work in order to study the base electrode in more detail as presented in Sec. 6.4. Both types of measurements, ultraviolet and X-ray photoelectron spectroscopy (UPS and XPS), use the photoelectric effect. They cover different energy ranges and have different penetration depths into the material. For that reason, XPS typically investigates deep lying core levels whose energy shifts according to the atomic net charge determined by their chemical bonding. However, these electrons mostly do not take part in the chemical bond itself, so that the shift is small (ca. 1 eV). In contrast to that, UPS is employed to measure the distribution of states close to the Fermi level. The principle is schematically shown in Fig. 4.7. Monochromatic electromagnetic radiation with the energy $h\nu$ excites electrons near the surface of the sample. All electrons with a binding energy E_B smaller than the energy of the photons are released with a kinetic energy

$$E_\mathrm{kin,S} = h\nu - E_\mathrm{B} \tag{4.7}$$

and some of them can leave the surface into the direction of detector where the measured kinetic energy $E_\mathrm{kin,Det}$ is increased by an acceleration voltage V_a, resulting in a better signal-to-noise ratio. The kinetic energy of the electrons is further influenced by a possible built-in potential between the sample (W_S) and the detector (W_D), given by

$$eV_\mathrm{bi} = e(W_\mathrm{S} - W_\mathrm{Det}) \tag{4.8}$$

arising from the fact that they are externally shorted and thus have an equal Fermi energy E_F. As a consequence, the kinetic energy of the electron

$$E_\mathrm{kin,Det} = E_\mathrm{kin,S} + eV_\mathrm{a} + eV_\mathrm{bi} \tag{4.9}$$

differs between the sample and the detector. Since the energy of the radiation is well known, the binding energy of the electrons E_B can be determined. XPS is performed with Al K$_\alpha$ radiation

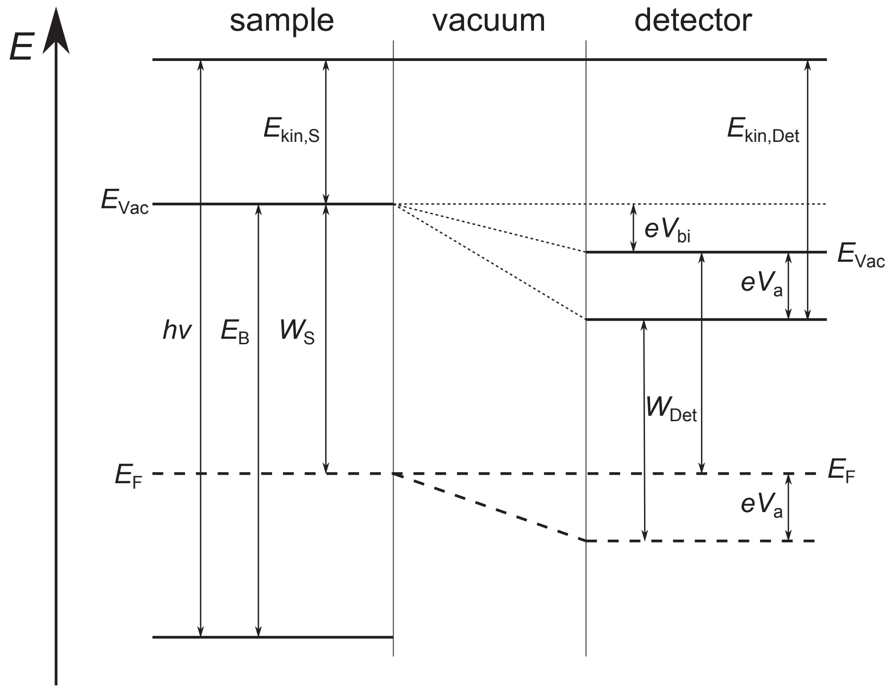

Figure 4.7: Schematic energy diagram, demonstrating the function of UPS and XPS

($h\nu = 1486.6\,\mathrm{eV}$), whereas for UPS, He-I radiation ($h\nu = 21.22\,\mathrm{eV}$) is used [53]. Combining Eq. 4.7 and 4.9 results in

$$E_{\mathrm{B}} = h\nu + eV_{\mathrm{a}} + eV_{\mathrm{bi}} - E_{\mathrm{kin,Det}} \quad , \tag{4.10}$$

representing the relation between binding energy of an electron state in the sample and the measurable kinetic energy at the detector. Nevertheless there are still unknown parameters, e.g. the built-in potential and thus the vacuum level position in the sample. For that reason, electrons are investigated for which $h\nu \sim E_{\mathrm{B}}$ applies, leading to the minimal measurable kinetic energy $E_{\mathrm{kin,Det,min}}$ at the detector. Since electrons with higher binding energies cannot be released, an abrupt breakup of the signal appears towards lower kinetic energies, associated with the high binding energy cutoff (HBEC), so that

$$E_{\mathrm{kin,Det,min}} = eV_{\mathrm{a}} + eV_{\mathrm{bi}} \tag{4.11}$$

can be used to determine the built-in potential and thus the vacuum level of the sample. Further, it is possible to calculate the work function of the detector by measuring a metal since its electrons with the lowest binding energies are located at the Fermi level, so that E_{B} is equal to W_{S}. Then, Eq. 4.10 reads

$$E_{\mathrm{kin,Det,max}} = h\nu + eV_{\mathrm{a}} - W_{\mathrm{D}} \tag{4.12}$$

where $E_{\mathrm{kin,Det,max}}$ is the highest measurable kinetic energy of the electrons at the detector.

With that knowledge, the work function of the sample can be determined with respect to its vacuum level, as given by Eq. 4.8. Similarly, the ionization potential of an organic semiconductor is determined via

$$I_\mathrm{p} = h\nu + eV_\mathrm{a} + eV_\mathrm{bi} - E_\mathrm{kin,Det,max} \tag{4.13}$$

By comparing the ionization potential of a semiconductor and the work function of a metal W_M in contact with it, one can measure the hole injection barrier

$$\Delta E_\mathrm{HIB} = I_\mathrm{p} - W_\mathrm{M} \tag{4.14}$$

Finally, the calculation of an electron injection barrier (EIB) is not directly accessible via UPS but using the transport gap E_g between HOMO and LUMO, an appropriate value

$$\Delta E_\mathrm{EIB} = E_\mathrm{g} - \Delta E_\mathrm{HIB} \tag{4.15}$$

can be obtained [320]. In order to determine the energy positions from measured spectra, a linear extrapolation of the slope to the background is done. Further details about the measurement setup and the evaluation of the data can be found elsewhere [321, 322].

4.3.5 Thermal imaging

The temperature distribution of the electrically driven devices is examined via an infrared (IR) camera VarioTHERM head II (JENOPTIK AG) with a macro lens.[3] The sensor is sensitive to wavelengths from 1.8 μm to 5 μm and the camera is cooled by a Stirling cooler in order to improve the measurement resolution down to 0.1 °C at 30 °C. It is important to be aware of the transmissive spectra of the materials employed. The glass substrate as well as the encapsulation glass show high transmittance up to 2.7 μm [318]. Thus, both permit a view onto the device. C_{60} has a high transmittance in the sensitive wavelength range, so that a calibration for this material is not practical [318, 323]. However, in that way, the signal from an underlying electrode is less disturbed. To calibrate the camera, a sample is embedded into a massive copper block with a slit above the encapsulation glass. Within the copper block, two temperature sensors are included, one below and one above the sample. The temperature difference detected by the sensors remains below 0.1 K. Since the sample is located between the two temperature sensors, the temperature of the device must be in between, and thus it is well known. The infrared camera is calibrated after the sample is set to 343 K (70 °C) using a heat plate in order to achieve an agreement of the applied temperature and the temperature measured by IR emission. Calibration is done for the Al electrode of the sample, having the same temperature as the organic layer underneath due to the extremely small thickness of the layer [318]. Since the resulting calibration factor is applied to the whole image, the temperature values in areas containing exclusively C_{60} are incorrect. To avoid measuring IR radiation emitted by the camera and reflected by the sample, the camera is tilted by a small angle with respect to the sample normal. Thus, the thermal images are slightly out of focus at the right and the left side.

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[3] Setup is kindly provided by Fraunhofer COMEDD, Dresden

4.4 MATERIALS USED IN C_{60} TRIODES

4.4.1 Buckminsterfullerene C_{60}

The vertical organic triodes, built in this work, are using Buckminsterfullerene[4] as the main semiconducting material. It is a unique molecule, having a spherical arrangement of 60 C atoms, so that its sum formula reads C_{60}. Similar to a football the atoms are located in a way producing a truncated icosahedron with 20 hexagons and 12 pentagons. The molecule is shown in Fig. 4.8 a).

The idea of a spherical carbon molecule has been mentioned for the first time by Osawa and Yoshida in 1970/71 [325,326]. Unfortunately, these works were written in Japanese and published in Japan, so that they drew less attention. The experimental discovery followed in 1985 by Kroto and coworkers [327].[5]. They used a laser to vaporize graphite and were able to detect clusters of carbon with a distinct number of atoms by time-of-flight mass spectroscopy. The breakthrough of C_{60} in research and application has been initiated by Krätschmer at al. in 1990 who found a method to synthesize C_{60} in large quantity at affordable costs [329]. Their finding triggered a wave of high impact publications in the '90s [324, 330–333]. For example, Sariciftci et al. showed that a photoinduced electron transfer occurs between a polymer and a C_{60} layer which finally resulted into the first C_{60} solar cell [334, 335]. Nowadays, C_{60} has become a standard material for small molecule organic solar cells [336–338]. In 1995, Haddon et al. demonstrated the first C_{60} thin film transistor. The many applications and new material properties of C_{60} have been summarized in several reviews [339–341]. In this work, various aspects of this molecule are of interest ranging from morphology and the electronic configuration to charge transport and stability in molecular layer. This points will be discussed in the next paragraphs.

C_{60} has a molar mass of 720 u, corresponding to 720.642 g/mol. The diameter of the molecule is found to be 7.1 Å [342]. There are different length between neighboring carbon atoms. The edges between two rings of six carbon atoms ((6,6) bond) have a length of 1.39 Å and rely on conjugated C-C bonds whereas the edges joining rings with six and five atoms ((6,5) bond) are 1.44 Å long [340]. C_{60} has a high thermal stability, showing a decomposition at temperatures above 1250 K [343]. At room temperature, C_{60} films have a close-packed, face-centered cubic (fcc) unit cell with a lattice constant of 14.2 Å [344]. The density of C_{60} is thus 1.67 g/cm^3. However, Heiney et al. showed that below 249 K, the orientation changes to a simple cubic lattice due to a first-order phase transition [345–347]. Sometimes, the phase transition is also observed at temperatures up to 260 K which might be related to sample preparation [348]. An abrupt increase in the lattice constant accompanies the reorientation [349, 350]. The electrical conductivity decreases by a factor of about one order of magnitude [348, 349, 351–354]. Furthermore, the heat capacity changes [352, 355]. In thin films of C_{60}, the consequences of the phase change are not consistently described in literature [356–359]. A phase transition might occur, but depending on the crystallite size and the charge carrier concentration, the change in conductivity could be overlaid by other effects.

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[4] The molecule is named after the american architect Richard Buckminster Fuller (1895 - 1983) whose spherical buildings are resembling [324].

[5] Robert F. Curl, Jr., Sir Harold W. Kroto, and Richard E. Smalley received the Nobel prize in chemistry in 1996 [328]

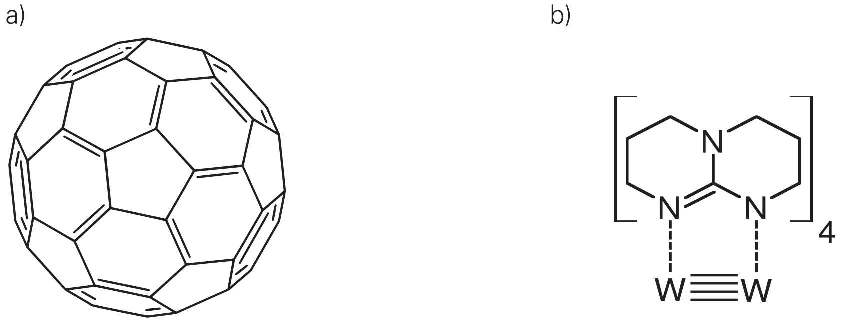

Figure 4.8: Structure formula of a) a C_{60} molecule. b) a $W_2(hpp)_4$ molecule. For clarity, only the front part of the spherical C_{60} molecule is shown.

Although C_{60} consists of several carbon rings with 5 or 6 atoms, it is not a fully aromatic molecule, meaning that electrons would be completely delocalized over the surface of the molecule. There is rather a network like structure of π-bindings which enable charges to redistribute on the molecule. For example, in the LUMO configuration, electrons align along the carbon pentagons [360, 361]. Nevertheless, the spherical shape of C_{60} ensures a high overlap of molecular orbitals between adjacent molecules, supporting intermolecular charge transfer [362]. The electronic states of C_{60} have been numerically studied by several groups [363–373]. The occupied molecular orbital with highest energy is five times degenerate, whereas the next higher state which is not occupied has a threefold degeneracy. This is the reason why C_{60} can accept up to six electrons in a solvent [374]. In turn, one can calculate the density of states for the LUMO as $8.4\text{x}10^{21}$ $1/\text{cm}^3$ when accounting for the mass of one molecule density of the material. Experimental studies by means of UPS and inverse photoelectron spectroscopy have revealed an energy bandgap of 2.3 eV [331, 341, 375, 376]. The HOMO level is located at 6.3 eV and the LUMO level 4.0 eV below the vacuum level [377]. The Fermi level of nominally intrinsic C_{60} is 1.7-1.8 eV above the HOMO level onset at an energy of ca. 4.4-4.5 eV and thus closer to the LUMO level which might correlate with the different degeneracy of HOMO and LUMO levels [375]. As an allotrope of carbon, C_{60} is considered to be inorganic. Nevertheless, it is a molecule with a HOMO and LUMO level, exhibiting a Gaussian DOS which is a typical feature of an organic semiconductor [21, 375] so that it can be treated accordingly. The standard deviation σ of the Gaussian DOS is about 0.25 eV [52, 375].

C_{60} is a predominantly n-type material. Reasons are the deep lying LUMO level of C_{60} which allows common metals like Ag, Au, and Al to form low electron injection barriers, so that sufficient electron injection is possible [378, 379]. As a further consequence, n-type doping can be realized either by alkali metals or by molecular dopants [332, 380, 381]. However, even without doping, the Fermi level of nominally intrinsic C_{60} is already shifted towards the LUMO levels. Instead, it is difficult to realize contacts to C_{60} with low hole injection barriers. Lee et al. have recently shown p-type behavior in OFETs using MoO_3 as dopant, but the hole mobility does not exceed 10^{-2} cm^2/Vs [382]. Although time-of-flight measurements in single crystals reveal that charge carrier mobilities around 1 cm^2/Vs are reached by electrons and holes, they can differ in polycrystalline C_{60} thin films [383]. For example, Könenkamp and coworkers demonstrated electron mobilities above 1 cm^2/Vs, but hole mobilities remain nearly four orders of magnitude lower [384].

Doping can change he conductivity of C_{60} by many orders of magnitude. Whereas an undoped single crystal C_{60} has an electrical conductivity lower than 10^{-14} S/cm at room temperature, thin films do typically conduct up to about 10^{-7} S/cm [351, 385, 386]. In contrast to that, by molecular doping very high conductivities of ca. 5 S/cm are achieved [381]. The change in conductivity is accompanied by a change in its temperature activation. Undoped C_{60} has an activation energy of the conductivity in the range of 0.5 eV [354, 385, 387]. However, highly doped layers exhibit values down to 50 meV which can be explained by the shift of the Fermi level towards the transport level [54, 380, 381].

A special property of C_{60} arises when it is doped with alkali metals, such as cesium, potassium, or calcium. These metal atoms can be incorporated into the C_{60} crystal lattice without destroying the crystallinity. Doped with potassium, extremely high electrical conductivities of 500 S/cm are reached [332]. Interestingly, at temperatures close to absolute zero, such layers become superconductive [331, 333, 388, 389]. Further, it is possible that up to six metal atoms per C_{60} molecule are intercalated, resulting in a complete filling of the LUMO levels by electrons [388, 390].

The transport in C_{60} can be described by temperature activated hopping arising from the Gaussian DOS [21, 54, 384, 386, 391, 392]. A typical feature thereof is an increasing mobility with charge carrier concentration and electric field [386, 393]. In order to correctly describe the transport at low charge carrier concentration, one has to account for trap states [54]. For example, Mehraeen et al. use an exponential trap distribution, ranging from the center of the Gaussian DOS into the energy gap to fit the experimental data by simulation. However, in the case of high charge carrier concentration, e.g. due to doping, these trap states are filled and neutralized [54, 55].

Charge transport has been further studied in terms of field-effect mobility in C_{60} OTFTs. Here, the electron charge carrier mobility is typically in the range of 0.1 to 1 cm^2/Vs [55, 394–399]. Depending on the surface treatment of the gate dielectric in a bottom gate configuration, values up to 4.9 cm^2/Vs can be measured [400–403]. By additionally heating the substrate during the deposition of the C_{60} layer in order to realize larger crystal grains, electron mobilities of up to 6.5 cm^2/Vs have been found [394, 395, 404–406]. However, Monte Carlo simulations by Kwiatkowski et al. suggest that the mobility hardly depends on the size of the C_{60} grains which they explain with the fact that the spherical shape of the C_{60} molecule always allows for a sufficient contact to neighboring molecules even at strong disorder [362].

Buckminsterfullerene molecules are not stable under ambient conditions. Single crystals and thin films are affected by oxygen and water [353, 407, 408]. Even small amounts of oxygen, 2 ppm in nitrogen atmosphere or a partial pressure of 2×10^{-6} mbar in vacuum, are sufficient to adversely affect the electrical properties of C_{60} [409, 410]. The speed of the degradation depends on the diffusion of oxygen and water into the material. For example, a 50 nm thick layer degrades within 10 min [410]. However, lateral diffusion of oxygen and water in C_{60} thin films with a width in the range of 100 µm to 1 mm needs several hours, so that the changes of the electronic properties slow down accordingly [411, 412]. There are several effects taking place upon exposure to oxygen. The C_{60} lattice contains interstices which are able to take up gas molecules without changing the crystal structure [413]. Intercalation of oxygen at these positions can be understood as physisorption. As a result, shallow trap states form, immediately decreasing the conductivity [353, 387, 407]. However, annealing in vacuum or nitrogen atmosphere at temperatures above 100 °C removes the intercalated oxygen molecules and restores the electrical conductivity [414, 415]. The situation changes if C_{60} exposed to oxygen is irradiated by visible or ultra violet light which supports an irreversible chemical reaction [416, 417]. Tsetseris and Pantelides calculate possible reaction products by density functional theory. They found that oxygen atoms can be incorporated by breaking either a (6,5) or a (6,6) bond which might happen more than one time on a single molecule, or chemically adsorbing an O_2 molecule by a (6,6) bond [408]. Oxygen is also able to build intermolecular bridges by connecting two C_{60} molecule with one or two oxygen atoms. Another reason for degradation of C_{60} is stronger annealing if the sample is stored in oxygen rich atmosphere or has been already exposed to air [418]. Above 470 K, oxide-carbon bonds form, revealed by an oxygen uptake equivalent to 12 oxygen atoms per C_{60} molecule, so that C_{60} decomposes into fragments [419]. At higher temperature, starting with ca. 570 K, C_{60} molecules are almost destroyed, mainly by reacting into carbon-oxygen compounds such as CO and CO_2 [420]. Besides the reaction with molecular oxygen, ozone O_3 is found to degradate C_{60} [421]. Thus, protection of C_{60} devices from ambient conditions is essential for a long operation time. This can be done by using a glass encapsulation as realized in this work, or by deposition of barrier layer protecting against gas and moisture [422, 423].

The Buckminsterfullerene used in this work is purchased from Creaphys GmbH (Germany) in sublimed grade. Several groups have investigated the vapor pressure of C_{60} at different temperatures. In a temperature range of 300 °C to 350 °C, a vapor pressure of $1\text{x}10^{-6}$ mbar is achieved [424–428]. Here, the material is thermally evaporated at a crucible temperature between 380 °C to 430 °C and at a pressure of 10^{-7} mbar. The deposition rate at the position of the substrate is 1 Å/s. Chen *et al.* showed that in a nitrogen atmosphere above 500 °C, a clear weight loss is detectable [420]. At normal pressure, the evaporation temperature should be strongly increased [428]. However, these measurements reveal that solid C_{60} thin films are thermally stable up to temperatures at which most of the organic semiconducting materials would have already been sublimed. Thus, C_{60} is a potential candidate for electronics allowing for elevated self-heating [318]. Further, related properties include a thermal conductivity of 0.4 W/m/K [429] and a thermal expansion coefficient of ca. $20\text{x}10^{-6}$/K [430, 431]. The dielectric constant of the intrinsic material is about 4.4 to 5 [323, 411, 432].

4.4.2 Tungsten paddlewheel $W_2(hpp)_4$

The molecule tetrakis(1,3,4,6,7,8-hexahydro-2H-pyrimido[1,2-a]pyrimidinate)ditungsten (II) has the sum formula $C_{28}H_{48}N_{12}W_2$ and is used as the main n-dopant material in this work, called $W_2(hpp)_4$ (purchased from Novaled AG, Germany). Its name is often denoted as tungsten paddlewheel, originating from its geometry: In the core, there are two tungsten atoms with a strong quadruple bond, forming the center of four ligands of 1,3,4,6,7,8-hexahydro-2H-pyrimido[1,2-a]pyrimidinate (hpp, $C_7H_{12}N_3$) arranged similar to the arms of a paddlewheel [433, 434]. The first synthesis of this material has been made by Cotton and coworkers in 2002 [435]. $W_2(hpp)_4$ is a unique molecule since it has an ionization energy of 3.51 eV, below the value of caesium. Therefore, electrons are easily transferred to molecules with high electron affinity e.g. C_{60} [433]. This can be understood as a redox reaction, making $W_2(hpp)_4$ an ideal n-dopant for organic semiconductors. Menke *et al.* demonstrated very high conductivities of 4 S/cm in co-evaporated thin films of C_{60} with $W_2(hpp)_4$ [380]. The molar mass of the molecule is 920.44 g/mol and thus it is somewhat heavier than C_{60}. $W_2(hpp)_4$ forms crystals with a triclinic lattice cell where the lattice angles α, β, and γ are at least higher than 70° [433]. The lattice constants are *a*, *b*, and *c* are in the range of 8 Å and 10 Å, so that this molecule has a smaller volume of the unit cell than C_{60}. As a consequence, $W_2(hpp)_4$ has a higher density (1.988 g/cm^3) in comparison to the Buckminsterfullerene caused by a denser packaging of heavier molecules. Although there are no studies on the morphology of mixed layer of C_{60} and $W_2(hpp)_4$, the smaller molecules of tungsten paddlewheel are expected to disturb the C_{60} lattice only weakly.

The low ionization energy also produces along some drawbacks. $W_2(hpp)_4$ readily reacts with oxygen and thus has to be transferred into the vacuum chamber without any air exposure [433]. Devices using the resulting n-doped layer are not air-stable and need additional encapsulation even though it is found that a part of the $W_2(hpp)_4$ molecules are passivated if doped into a C_{60} matrix layer within a certain time frame [52]. Nevertheless, if an inert environment is ensured, the tungsten paddlewheel has a good thermal stability. It can be sublimed between 220 °C and 250 °C at a pressure around 10^{-4} mbar [435] and shows no decomposition at temperatures of at least 300 °C [436]. For example, preparation of samples by thermal evaporation of $W_2(hpp)_4$ as used in this work results in crucible temperature during evaporation between 178 °C and 222 °C at a pressure around 10^{-7} mbar. Devices with crossbar electrodes and an n-doped/intrinsic/n-doped layer configuration containing $W_2(hpp)_4$ show operational stability up to temperatures above 200 °C [318, 437]. The positive features of this molecule prevail, so that it is nowadays used in organic solar cells [438–441] and vertical organic triodes [181] as n-doped injection layer. Another field of application is the tuning of operation parameters in OFETs, like contact resistance and threshold voltage [80, 442].

4.4.3 Aluminum and its oxides

Special attention is given here to the metal aluminum (Al) which is used as the material for the base electrode of the vertical organic triode. Due to its growth on C_{60} and its characteristic self-passivating oxide formation, it contributes in an essential and unique way to the overall device function, as will be discussed in the results chapters 5-9. The usage of aluminum in electronic applications and as a light weight construction or packaging material led to a huge number of investigations. Important properties are reviewed in Ref. [443] and [444], as summarized in the following. Aluminum, the element with the atomic number 13, has an electron configuration of [Ne] $3s^2$ $3p^1$ and a mass of 26.981 u. At room temperature, it crystallizes in a fcc lattice structure with 4.0 Å as the lattice constant of the cubic unit cell. With a density of 2.70 g/cm^3, Al is a relatively light metal. It has good electrical and thermal properties, so that it is widely used in semiconductor electronics. The specific electrical conductivity is 2.65×10^{-8} Ωm and the thermal conductivity is 237 W/m/K. The thermal expansion coefficient is 23×10^{-6}/K, comparable to that of C_{60}. In this work, aluminum is used as an electrode, fabricated by thermal vapor deposition. The material is purchased from Kurt J. Lesker Company (USA) with a purity of 99.999 %. Evaporated pellets have a diameter and a length of 1/8" each. The melting point of aluminum is reached at 933.5 K and boiling begins as 2743 K. For Al nanoparticles, a melting point depression is observed, reducing the melting point by up to 140 K for particles with 20 Å [445–447].

Aluminum oxidizes to three different species by reaction with water or oxygen. Besides aluminum oxide Al_2O_3, there exist aluminum oxide-hydroxide $AlO(OH)$ and aluminum trihydroxide $Al(OH)_3$.

They differ in their degree of hydration, starting from aluminum oxide which incorporates no water up to aluminum hydroxide. All these material form crystalline structures which result in different properties and nomenclature depending on the crystal system.

Aluminum oxide has a hexagonal crystal lattice, and its mineral is called corundum. It is a highly transparent material in the wavelength range of the visible radiation [448]. The reason can be found in the large band gap energy of 8.8 eV which prevents any absorption of light. If there are some impurities with traces of a metal, corundum is well known as a gem, e.g. ruby or sapphire [449]. Pure aluminum oxide is a highly insulating materials and further exhibits an excellent dielectric breakdown strength of 5 MV/cm for a large layer thickness and up to 50 MV/cm for layer of thicknesses in the nm range [450, 451]. Furthermore, it has a rather high permittivity of 8 to 9 [451]. This properties makes aluminum oxide an ideal candidate as an insulating gate dielectric in field-effect transistors [110, 452, 453]. Al_2O_3 originates from reaction of aluminum with either oxygen

$$4\mathrm{Al} + 3\mathrm{O}_2 \rightarrow 2\mathrm{Al}_2\mathrm{O}_3 \tag{4.16}$$

or water

$$2\mathrm{Al} + 3\mathrm{H}_2\mathrm{O} \rightarrow \mathrm{Al}_2\mathrm{O}_3 + 3\mathrm{H}_2 \tag{4.17}$$

and the resulting self-limiting layer thickness of the native oxide can be adjusted by temperature and pressure [451, 454, 455]. Further methods to realize aluminum oxide are atomic layer deposition for realization of thin and uniform layers as well as anodic oxidation which leads to thicker layers but with potential formation of pores [456, 457].

There are further possible reactions with water, resulting in aluminum hydroxides [449]. The reaction

$$2\mathrm{Al} + 6\mathrm{H}_2\mathrm{O} \rightarrow 2\mathrm{Al(OH)}_3 + 3\mathrm{H}_2 \tag{4.18}$$

leads to the formation of aluminum trihydroxide which crystallizes in three different lattices. The most common form is the mineral gibbsite with a monoclinic unit cell. Other types are bayerite and nordstrandite with a hexagonal or a triclinic lattice, respectively. Furthermore, aluminum oxide-hydroxide forms by the following reaction

$$2\mathrm{Al} + 4\mathrm{H}_2\mathrm{O} \rightarrow 2\mathrm{AlO(OH)} + 3\mathrm{H}_2 \tag{4.19}$$

for which two different kinds of crystal growth exists. Both, boehmite and diaspore, have an orthorhombic lattice system, and in comparison to the aluminum trihydroxide less water is incorporated. It has been found that depending on temperature and pressure, both types of aluminum hydroxide are convertible into each other:

$$\mathrm{AlO(OH)} \leftrightarrow \mathrm{Al(OH)}_3 \tag{4.20}$$

as described in Ref. [449]. At high temperatures, 725 K to 1400 K, depending on the base material, aluminum hydroxides ultimately decompose into aluminum oxide by release of water.

Upon air exposure, aluminum quickly forms an oxide on its surface which saturates at a thickness reaching 2-3 nm [454, 458–463]. This oxide layer is not pervious to oxygen or water so that a further growth is inhibited. However, there might be a slight diffusion through this layer, resulting in an ongoing increase of the oxide layer thickness over years, so that the layer thickness could increase further to 4-5 nm if exposed to air. Thus, this native oxide has a self-passivating character, making it resistive to corrosion. Rippard *et al.* demonstrated that the oxide thickness is very homogeneous and highly free of pinholes [464]. McCafferty and Wightman have investigated the composition of such a native aluminum oxide layer [465]. They assume that an aluminum oxide layer forms in direct contact to the metal which is responsible for the limited oxide growth. On top, a region of hydroxylated aluminum is present with a thickness of 5 to 8 Å. Furthermore, it is reasonable that water molecules are adsorbed on the surface. In that sense, aluminum exposed to air is composed of differently oxidized layers, so that its stoichiometry is unknown. Therefore, the native oxide layer is often referred to AlO_x as also used in this work. As a consequence, AlO_x layers differ in their properties from Al_2O_3, e.g. a permittivity as low as 4.5 can occur, somewhat smaller than that of aluminum oxide [451].

Thin or ultrathin aluminum oxide layers are employed or considered for several applications, e.g. as tunnel junctions. Josephson tunnel junctions can be fabricated by embedding a thin oxidized layer of aluminum between two superconducting materials [466, 467]. Furthermore, magnetic tunnel junctions are built by such a layer structure with ferromagnetic materials as electrodes [464, 468]. In single electron transistors, AlO_x is used as a tunnel barrier between small conducting islands with nanometer feature size. [469–472] Thus, tunneling of single charges can be investigated. Further applications include infrared detectors with an antenna-coupled metal-oxide-metal diode [473]. Here, the tunnel junction realized by the AlO_x layer acts as a rectifier due to its nonlinear current-voltage characteristic [474].

The popular use of AlO_x as a tunnel junction already indicates that charge transport in this insulating layer is governed by tunneling processes [475, 476]. Depending on the thickness and the defect density, direct tunneling or resonant and inelastic tunneling are dominant. Gloos and coworkers assume that at least for a thickness below 1 nm, mainly direct tunneling occurs, meaning that the charge transport is determined by the thickness and the height of the oxides energy barrier [451]g. Additionally, image charge induced barrier lowering occurs which is most pronounced for thin layers [88]. At higher layer thicknesses, defects lead to localized states, enabling trap-assisted tunneling [451, 477].

AlOx is increasingly applied as a gate dielectric in thin film transistors. This material exhibits leakage current densities of 100 to 1000 mA/cm^2 at 1 V and shows a capacitance per area of ca. 2.5 µF/cm^2 [476,478,479]. Although such values might still be acceptable for inorganic transistors based on complementary metal-oxide-semiconductor technology, organic field-effect transistors require much lower gate leakage in order to achieve high on/off ratio and a large current gain [84]. A typical approach to reduce gate leakage is the treatment of the aluminum electrode in oxygen plasma, leading to a certain increase in oxide thickness, and the resulting current densities do not exceed 1 mA/cm^2 at 1 V [480, 481]. It has been further shown that a self-assembled monolayer of a long carbon chain molecule with a phosphonic acid-based anchor group attaching to the surface of AlO_x layer significantly reduces the gate leakage current to 10^{-5} mA/cm^2 and the capacitance per area to about 800 nF/cm^2 [110, 480].

4.4.4 Spiro-TTB

In this work, an insulating material is used in order to restrict the current flow in the vertical organic triodes to a defined active area. For that reason, a material is needed which is compatible with the available processing techniques such as thermal evaporation and the sample treatments like annealing at 150 °C. A suitable material is 2,2',7,7'-tetrakis(N,N'-di-p-methylphenylamino)-9,9'-spirobifluorene (purchased from Lumtec Technology Corp., Taiwan) [482]. The short name is Spiro-TTB and it has the sum formula $C_{81}H_{68}N_4$ [482, 483]. Commonly, the material is employed as a hole transport layer in OLEDs [106, 484, 485]. One reason is that the HOMO onset level lies around 5.1 eV with respect to the vacuum level, allowing to dope this material and to realize proper hole conduction. However, the material can also be used for different purpose: It can act as an electron blocking layer. This behavior can be also utilized in combination with C_{60} in vertical organic triodes. By comparison of the LUMO levels, electrons have to overcome an energy barrier of ca. 2 eV at the interface C_{60}/Spiro-TTB [485]. Since interface dipoles at organic/organic interfaces of intrinsic layers are typically smaller than 1 eV, a sufficiently high energy barrier can be assumed to efficiently block the electron flow [67, 68, 486]. There is no report about electron mobility of Spiro-TTB in the literature yet, but the hole mobility of $5.7\text{x}10^{-5}\text{cm}^2/\text{Vs}$ suggests that the electron mobility might be on a similar low level [482]. Thus, even if there are no electron injection barriers between C_{60} and Spiro-TTB, the current will be reduced by several orders of magnitude due to the lower charge transport in this material. A further important property is the thermal stability since the insulating layer must withstand the annealing of the vertical organic triodes done at 150 °C after fabrication. Salbeck and coworkers have investigated several spiro compounds and listed their thermal properties in Ref. [23]. Spiro-TTB has a glass transition temperature of 146 °C, close to the annealing temperature. This temperature is defined as the initiation of the transition from a solid phase to a liquid phase in which the material is in a molten state. It will be verified in Sec. 8 whether the material can withstand the annealing without morphological changes. The recrystallization of Spiro-TTB starts at 192 °C, the melting at 293 °C, and decomposition begins at 510 °C. In that sense, Spiro-TTB has a comparably good thermal stability for an organic semiconductor. Furthermore, it is stable in air for at least for 4 months [482].

4.5 MATERIALS USED IN ORGANIC LIGHT-EMITTING DIODES

Organic Light-emitting Diodes (OLED) are fabricated using the pin technology [487]. Therefore, p-doped and n-doped layers next to the electrodes ensure proper injection of holes and electrons into the device at a low operation voltage. The material for the hole injection layer is N,N,N′,N′-tetrakis-(4-methoxyphenyl)-benzidine, called MeO-TPD (purchased from Sensient Technologies, USA). The p-doping of layer with this molecule is realized by F6-TCNNQ (2,2′-(perfluoronaphthalene-2,6-diylidene)dimalononitrile (purchased Novaled AG, Germany)) with a doping concentration of 2wt%. Injected holes are transported through a hole transport layer of N,N′-Di(naphthalene-1-yl)-N,N′-diphenyl-benzidine (NPB, purchased from Sensient Technologies, USA), simultaneously acting as a blocking layer for electrons. The layer configuration is similar for the electron transporting layers. A layer of 4,7-diphenyl-1,10-phenanthroline (BPhen, purchased from abcr GmbH & Co. KG, Germany) is doped with Cs (purchased from SAES Getters S.p.A., Italy) in a ratio of 1:1 and acts as the electron injection layer. Electrons are transported to the light-emitting zone via a layer of aluminum (III) bis(2-methyl-8-quninolinato)-4-phenylphenolate (BAlq, purchased from Sensient Technologies, USA). For the light-emitting layer, different material combinations are used in order to realize a red, green, and blue OLED. Blue light emission is enabled by mixing the host material 2,5,8,11-tetra-tert-butylperylene (TBPe, purchased from Lumtec Technology Corp., Taiwan) with 1.5wt% of the emitter molecule 2-methyl-9,10-bis(naphthalen-2-yl)anthracene (MADN, purchased from Lumtec Technology Corp., Taiwan). By using NPB as a host and iridium(III)bis(2-methyldibenzo[f,h]quinoxaline) (acetylacetonate) (Ir(MDQ)$_2$(acac), purchased from American Dye Source Inc., Canada) with mixing concentration of 10wt%, red light emission is realized. The green light emission is realized by a two layer system. The first layer consists of the host material 4,4′,4″-tris(N-carbazolyl)-triphenylamine (TCTA, purchased from Sensient Technologies, USA) mixed with 8wt% of fac-tris(2-phenylpyridine) iridium (Ir(ppy)$_3$, purchased from Sensient Technologies, USA). The same emitter molecule is further used with the host 2,2′,2″-(1,3,5-Phenylen)tris(1-phenyl-1H-benzimidazol) (TPBI, purchased from Sensient Technologies, USA) in order to fabricate the second layer. The devices are deposited on a glass substrate with prepatterned indium-tin-oxide electrodes and an aluminum top contact.

5 INTRODUCTION OF C_{60} VOTS

The work presented here is based on a Vertical Organic Triode using the small molecule C_{60} as the semiconducting material. As starting point, the fabrication of these C_{60} triodes is explained by introducing the layer stack and the essential treatments. This sample structure will be the basis for further investigations and improvements. In contrast to OFETs, Vertical Organic Triodes are a relatively young field and have been investigated only by a small number of scientific groups worldwide. Therefore, this chapter introduces the basic characteristics of this device and shows how to determine the most important parameters. Especially, the base sweep measurements and the common-base characteristics will give interesting insights into the device operation.[1]

5.1 SAMPLE PREPARATION

The structure of the triode is schematically shown in Fig. 5.1. The VOT is built by thermal vapor deposition in vacuum and structured by shadow masks (active area of $4\,\mathrm{mm}^2$). Processing details can be found in chapter 4. As semiconductor, the electron conductive material C_{60} with a thickness of 100 nm is used for bottom and top layer, realizing an n-type VOT. For top and bottom electrode, a combination of Al (50 nm) and Au (20 nm) is used. The aluminum part of the electrodes decreases the resistance of the electrode and ensures a proper wetting of the thin film on the glass substrate. The gold layer provides a sufficient electron injection into C_{60} and prevents the Al layer from oxidation.[2] The middle or base contact consists of a 15 nm thin Al electrode and is exposed to air for 15 min. Once the devices are completed with a second C_{60} layer and the top electrode, encapsulation in nitrogen atmosphere and annealing at 150 °C to 170 °C is done for 2 h. The effect of the annealing is shown in chapter 6 and the role of the oxidation process is discussed in chapter 7. A layer of C_{60} doped with the highly efficient n-dopant $W_2(hpp)_4$ (n-C_{60}) with a thickness of 20 nm is inserted to improve the injection by reducing the contact resistance [380]. The dopant is co-evaporated with C_{60} at a concentration of 2 wt%, leading to conductivities in

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[1] The work presented in this section is published in Ref. [181].

[2] Further studies have revealed that the use of 10 nm chrome instead of 20 nm Au leads to a comparable performance.

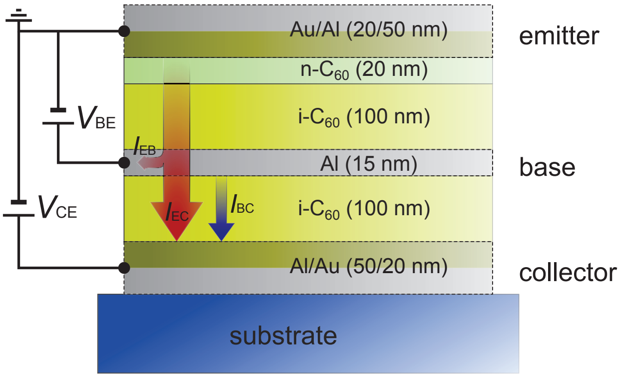

Figure 5.1: Structure of a C_{60} triode with a 15 nm thin permeable Al base electrode. An n-doped layer between the top electrode and the upper C_{60} layer ensures Ohmic injection into the device.

the range of 1 S/cm. Intrinsic layers of C_{60} without dopants are referred to as i-C_{60}. Detailed processing steps are explained in Sec. 4.1.

5.2 DIODE CHARACTERISTICS

First, the diode characteristics of the top and the bottom diode are discussed. Figure 5.2 presents the corresponding IV curves. The potential is applied to the base electrode. Depending on the measured diode, one outer electrode is grounded and the opposite electrode is floating (disconnected). Thus, electrons flow from the outer electrode into the base electrode, for positive voltages, called forward direction. This current corresponds to a leakage current from emitter to base I_{EB}, leading to a decrease of the current gain, if it would occur in a transistor configuration. At negative voltages (backward direction), current is injected at the base electrode, flowing to one of the outer electrodes. This BC leakage current I_{BC} determines the minimum collector current in the off-state of a VOT. Both types of leakage current are schematically shown in Fig. 5.1.

In forward direction, top and bottom diode have similar currents for small voltages ($< 0.5\,V$), but the top diode is able to reach slightly higher currents at voltages around 3 V. One reason might be the use of a doped injection layer underneath the top electrode. Nevertheless, the injection from the Au layer of the bottom electrode into the i-C_{60} layer is sufficiently high and both diodes can be used as the emitter diode of the VOT. In backward direction, the bottom diode has one order of magnitude lower currents compared to the top diode. For a VOT, the emitter diode is used in forward direction and the collector diode in backward direction so that the best combination is given by using the top electrode as the emitter. Then, the highest ratio between current at the emitter and BC leakage current can be expected. However, the opposite direction, using the bottom electrode as the emitter, still has a sufficient ratio between the forward direction of the bottom diode and the backward direction of the top diode, reaching three orders of magnitude at 3 V. Thus, both operation directions can be studied.

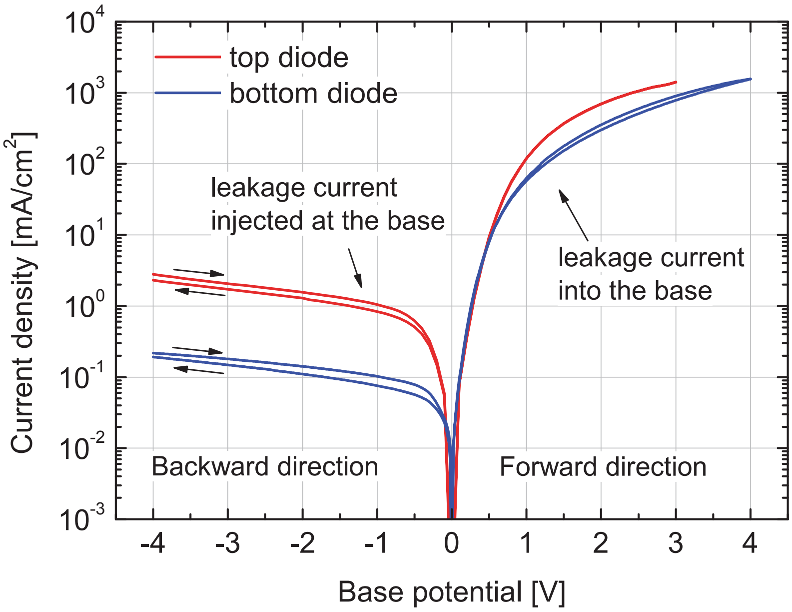

Figure 5.2: IV characteristic of top and bottom diode. The potential is applied to the base electrode, and top or bottom electrode are grounded. The contact which does not contribute is disconnected (floating). In forward direction, the measured current is corresponding to charges, directly flowing into the base electrode and representing an EB leakage current if the diode is used as emitter. In backward direction, electrons are injected at the base electrode and flow to the outer electrode, representing BC leakage current if used as the collector.

5.3 BASE SWEEP MEASUREMENT

Potential configuration The base sweep is the standard measurement to demonstrate the device function and to determine various device parameters. In a common-emitter configuration, a constant driving voltage V_{CE} is applied. For example, the emitter potential is 0 V and the collector potential is kept constant at the driving voltage of 3 V. The base potential is now varied to realize a minimum and a maximum collector current flow. Thus, the transistor switches between the on- and off-state. In comparison to a field-effect transistor, the base sweep is equivalent to a transfer characteristic (gate sweep) where the drain-source voltage is kept constant and the gate potential is varied. In the VOT, the base electrode is clearly assigned to be the control electrode by varying the charge flow through it. The other two electrodes, however, are arranged symmetrically to the middle electrode and have no predefined purpose. Therefore, the top electrode can be used as the emitter together with the bottom electrode as the collector or vice versa. Both measurements are presented in Fig. 5.3 for the transmitted electrons flowing downwards (a) or upwards (b) with respect to the substrate. The subsequent discussion and parameter evaluation refers to this measurement.

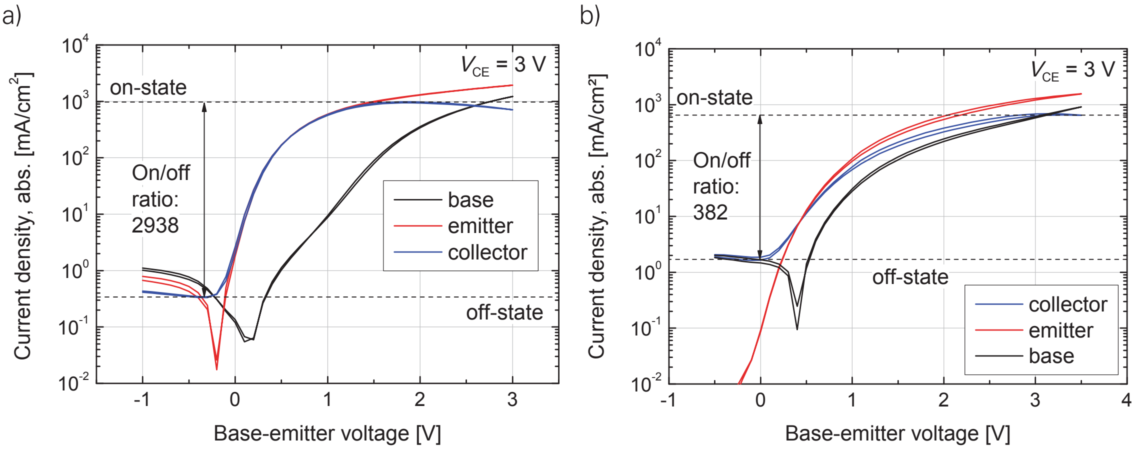

Figure 5.3: Base sweep measurement at a driving voltage of 3 V for a) the top electrode as the emitter or b) the bottom electrode as emitter. For both operation directions, a clear change in collector current density is revealed by varying the base-emitter voltage. Voltages are swept forward and backward within a time frame of 1-2 seconds in order to demonstrate reversible switching and only a small hysteresis.

Basic operation First of all, it has to be shown that the device works properly by demonstrating the collector current is modulated with a variation of the base-emitter voltage. In Fig. 5.3a), there is a clear dependence of the collector current density on the base potential, and sweeping forward or backward does not make a difference, i.e. there is a small hysteresis. Considering that

$$V_{\mathrm{CE}} = V_{\mathrm{BE}} + V_{\mathrm{CB}} = const. \quad , \tag{5.1}$$

the base-emitter voltage increases whereas the collector-base voltage simultaneously decreases. The fact that the collector current still increases, although the collector-base voltage decreases, indicates that the collector current is rather given by a transmission current through the base electrode than by an electron flow injected at the base contact. Furthermore, in the voltage range $0\,V < V_{\mathrm{BE}} < 1.5\,V$, both emitter and collector currents are almost identical, overlapping each other. Thus, it can be assumed that the collector current is realized by electrons injected at the emitter contact, and consequently, it must have been transmitted. Three qualitatively different regimes can be distinguished for a base sweep:

1. The base-emitter voltage is below 0 V: Both diodes (BE and BC) operate in backward direction, and the current flow through the device is suppressed.
2. The base-emitter voltage is larger than 0 V but smaller than the driving voltage: The BE diode is used in forward direction and the BC diode in backward direction, realizing ideal conditions for charge carriers to be transmitted.
3. The base-emitter voltage is larger than the driving voltage: Both diodes (BE and BC) operate in forward direction and the transmission current is suppressed by the oppositely directed electric field of the BC diode, or superimposed by charges injected at the collector.

The behavior of the base sweep measurement is similar whether the top electrode is used as the emitter or the bottom electrode (cf. Fig. 5.3). Thus, the transmission process is bidirectional.

Charge carriers can cross the base electrode from both sides without being extracted into it. Such a behavior can hardly be explained by a tunneling of hot-carriers through the base electrode, because this process is highly asymmetric due to the higher energy barrier from the base to the emitter layer than to the collector layer. Supporting this argumentation, it can be shown that for both operation directions, a transmission above 90% can be reached, as shown in Sec. 5.5 and Sec. 8.2. However, Spratt *et al.* have not reached transmission higher than 90% for a hot-electron transistor, utilizing a 10 nm thin Al base electrode [488]. Heiblum states that the maximum transmission (there: transfer ratio) is 0.9, as the mean free path of the electrons is in the range of the thickness of the base electrode, and thus too large [139]. A more appropriate explanation for the high transmission observed here is the existence of pinholes in the base electrode, allowing for direct contact of the upper and the lower i-C_{60} layer and for charge transmission in both directions.

The base sweep measurement further allows to determine the dominant type of charge carriers in this unipolar transistor. Independent of the potential configuration used, the outer electrode with the lower potential acts at the emitter for an n-type VOT. Then, the collector current increases with increasing base potential. In contrast, for a p-type VOT, the electrode with the higher potential is automatically the emitter and the collector current increases with decreasing base potential. For example, the C_{60} triode discussed here clearly shows a conduction of electrons. It cannot be excluded that holes are present in the device, but they have a negligible influence on the device performance.

Operation states The off-state is reached at a low base potential. Then, the base-emitter voltage is small or even negative which prevents current to be injected at the emitter and thus to be transmitted. At the same time, the collector-base voltage is highest and the residual collector current is given by the injection of charge carriers at the base. In Fig. 5.1, a blue arrow visualizes this backward current of the BC diode. For an ideal VOT, this current should be zero. If the base potential decreases further, also backward currents of the BE diode can be observed at $V_{\mathrm{BE}} < -0.2\,\mathrm{V}$ in Fig. 5.3a), flowing from the base to the collector. The collector current density in the off-state is below 1 mA/cm^2 which is still too high for some applications. For example, an OLED at this current density exhibits a luminance of more than 100 cd/m^2 which is the operating range for display applications [489]. If the active area of the VOT is not scaled to match the OLED characteristics, it will be important to drastically reduce the off-state current density.

In the voltage range $-0.2\,V < V_{\mathrm{BE}} < 0.5\,V$, the collector as well as the emitter current rise exponential. Here, the current flowing through the device can be strongly modulated by the base potential with a base current which is two orders of magnitudes lower. Thus, current amplification is demonstrated as a consequence of a high charge carrier transmission through the base electrode. Finally, the on-state is reached at a base-emitter voltage of 1.5 V, reaching collector current densities of about 1000 mA/cm^2. Such a current density would be sufficient to drive an OLED up to an extreme luminance of 10^5 cd/m^2 if the OLED withstands that [490]. At the same time, the driving voltage of the C_{60} triode is lower than the driving voltage of the OLED. In comparison with other approaches for vertical organic transistors with planar electrodes, the current density is one of the highest reported so far [168, 243, 262, 271, 280, 281]. Only for OFETs utilizing step-edge structures as the channel, higher effective current densities are reported [306], but they require a higher driving voltage and rely on a Si-Wafer as substrate, hindering the fabrication on foils. Higher base potentials as required for the on-state finally lead to a reduction of the collector current. While the emitter current permanently rises with increasing base-emitter voltage, the collector-base voltage, responsible for the conduction of transmitted charges to the collector, decreases. If the base potential is equal to that of the collector, charges are no more collected efficiently and the transmission is weaker. Then, injected charges at the emitter mainly get captured in the base electrode, leading to higher base than collector currents. In this regime, the VOT loses its current gain and cannot efficiently be used in applications.

5.4 DETERMINATION OF PARAMETERS

On/off ratio The on/off ratio is one of the most important parameters of a transistor device. It is defined as the ratio between the collector current in the on-state I_{On} and the one in the off-state I_{Off}, i.e.

$$\text{On/off ratio} = \frac{I_{\mathrm{On}}}{I_{\mathrm{Off}}} = \frac{I_{\mathrm{C,max}}}{I_{\mathrm{C,min}}} \quad \text{for} \quad V_{\mathrm{CE}} = \text{const.} \tag{5.2}$$

with $I_{\mathrm{C,max}}$ and $I_{\mathrm{C,min}}$ the highest and the lowest collector current. If the top electrode is used as the emitter and V_{CE} is 3 V, the on/off ratio reaches 2938, a value sufficiently high to further characterize the device. However, for an application, values larger than 10^5 to 10^6 are typically required to minimize the power consumption in the off-state and, e.g., for display applications to realize a large brightness contrast. Thus, further optimization has to concentrate on minimizing currents in backward direction of the BC diode and to check whether even higher on-state current densities can be achieved.

Threshold voltage The threshold voltage V_{th} corresponds to the base-emitter voltage above which the transistor becomes highly conductive. Figure 5.4 shows the collector current and its square root vs. the base-emitter voltage. Although there is no obvious reason for a quadratic law of the collector current in a base sweep, a corresponding region can be found where the square root of the collector current is linear, similar to an OFET. However, in contrast to an OFET, it is not possible to extract further information from that slope, e.g. the charge carrier mobility. The threshold voltage can still be estimated from the square root of the collector current by an extrapolation of the linear region to zero, resulting in a value of $V_{\mathrm{th}} = 0\,\mathrm{V}$ in this example. In a field-effect transistor, the threshold voltage describes the configuration when the channel region has no depleted parts anymore. This interpretation does not make sense for a VOT as long as the operation mechanism is still under investigation. Instead, the threshold voltage of a C_{60} triode has to be understood as the transition from the exponentially growing regime of the collector current to the regime where the collector current starts to saturate, finally reaching its maximum value in a base sweep measurement. Please note that this current saturation in the base sweep measurement is different from current saturation in general, e.g. as it might be obtained for the output characteristics.

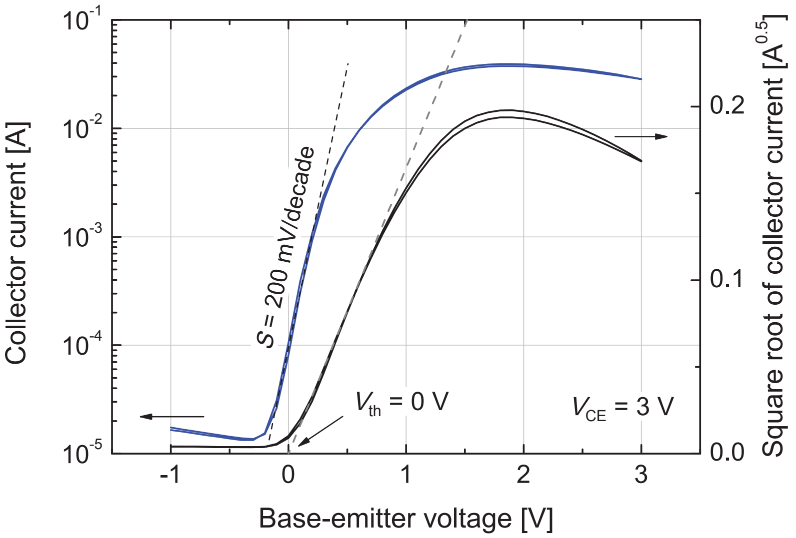

Figure 5.4: Determination of the threshold voltage and the subthreshold swing from the base sweep measurement. By extrapolation of the linear region of the square root of the collector current to zero, a threshold voltage of $V_{\mathrm{th}} = 0\,\mathrm{V}$ is estimated. In the range of this base-emitter voltage, a subthreshold swing of 200 mV/decade is realized.

Subthreshold swing The subthreshold swing characterizes the voltage which is needed in order to change the current flow of a transistor by one order of magnitude, defined as

$$S = \left.\frac{\partial V_{\mathrm{BE}}}{\partial(\log I_{\mathrm{C}})}\right|_{V_{\mathrm{CE}}=const.} \tag{5.3}$$

and determined in the subthreshold region where the collector current increase exponentially with the base-emitter voltage ($V_{\mathrm{CE}} < V_{\mathrm{th}}$). To guarantee a sharp transition from the off-state to the on-state, this value should be as small as possible. Thus, the subthreshold swing influences the voltage range in which a logic circuit can operate. The C_{60} triode has a minimum subthreshold swing of 200 mV/decade as visualized in Fig. 5.4a) which is above the theoretical limit of 60 mV/decade [3]. For comparison, best OFETs reach values around 100 mV/decade [110]. The subthreshold swing typically becomes smaller when the collector current is lower. However, at low current densities, a limitation is given by the current of the BC diode, flowing in backward direction, so that the subthreshold region is less pronounced in the measurement. It is reasonable to assume that the subthreshold swing could be even smaller if the on/off ratio would be much greater.

Transconductance Another important parameter is the transconductance or mutual conductance defined by

$$g_{\mathrm{m}} = \left.\frac{\partial I_C}{\partial V_{\mathrm{BE}}}\right|_{V_{\mathrm{CE}}=\mathrm{const.}} \tag{5.4}$$

which compares the modulation of the collector current by an incoming voltage signal at the base electrode. A high transconductance is necessary for amplifying small signals, e.g. for driving loudspeakers. For an OFET, the transconductance is proportional to the transit frequency as given by Eq. 3.10, and it can be assumed that a similar relation can be applied to VOTs. Thus, a high transconductance is a prerequisite for high switching speed. Fig. 5.5 presents the

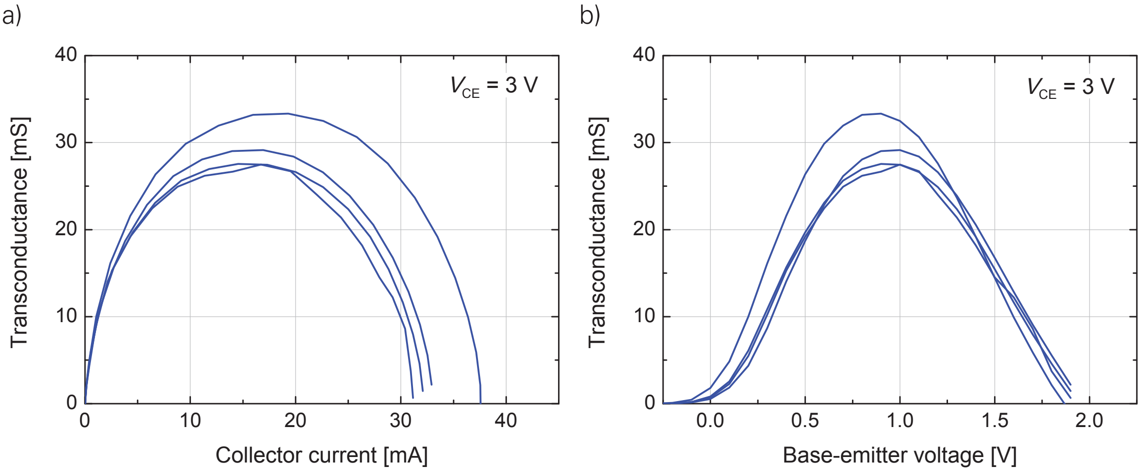

Figure 5.5: Transconductance for top electrode as the emitter as a function of a) collector current and b) base-emitter voltage.

transconductance of the base sweep in Fig. 5.3 over the collector current (a) and the base-emitter voltage (b). Maximum values in the range of 30 mS are reached at a collector current of 15 mA to 20 mA ($\sim$ 500 mA/cm^2) and a base-emitter voltage of 0.75 V to 1 V. For comparison, vacuum tube triodes have values in the range of 1 mS to 10 mS which nonetheless can, driven at high voltages of more than 100 V, be operated at a higher power than VOTs.

Transmission and current gain Determination of the current gain is fairly simple because one has to compare collector and base current. However, the situation is more complicated if a parasitic current I_{BC}, flowing in backward direction of the BC diode, superimposes the transistor characteristic. Then, calculated values are erroneous as long as $I_{BC} << I_T$ is not fulfilled. This is similar for the transmission which can be overestimated if the collector and the emitter current are compared directly. Thus, an evaluation is justified when the current given by the BC diode becomes much smaller than the collector current, so that it is mainly given by the transmission current: $I_C \sim I_T$. In Fig. 5.3a), this assumption holds true above a base-emitter voltage of 0.5 V where the collector current is at least two orders of magnitude higher than the current in the off-state. The corresponding direct transmission is shown in Fig. 5.6a) together with the equivalent current gains. Starting at 99.39%, the charge carrier transmission is continuously decreasing, but remains above 90% in the on-state at $V_{BE} = 1.5$ V so that in the whole operation range a current gain above 10 is realized. Up to a base-emitter voltage of 0.75 V, the current gain is above 100 and the collector current density in this range still exceeds 100 mA/cm^2. Such a current gain is comparable to the one achieved by an inorganic bipolar junction transistor.

A more reliable way to determine transmission and current gain relies on the use of their differential counterparts, namely the differential transmission

$$\alpha_{\text{diff}} = -\left.\frac{\partial I_C}{\partial I_E}\right|_{V_{CE}=const.} \tag{5.5}$$

and the differential current gain

$$\beta_{\text{diff}} = \left.\frac{\partial I_C}{\partial I_B}\right|_{V_{CE}=const.} \tag{5.6}$$

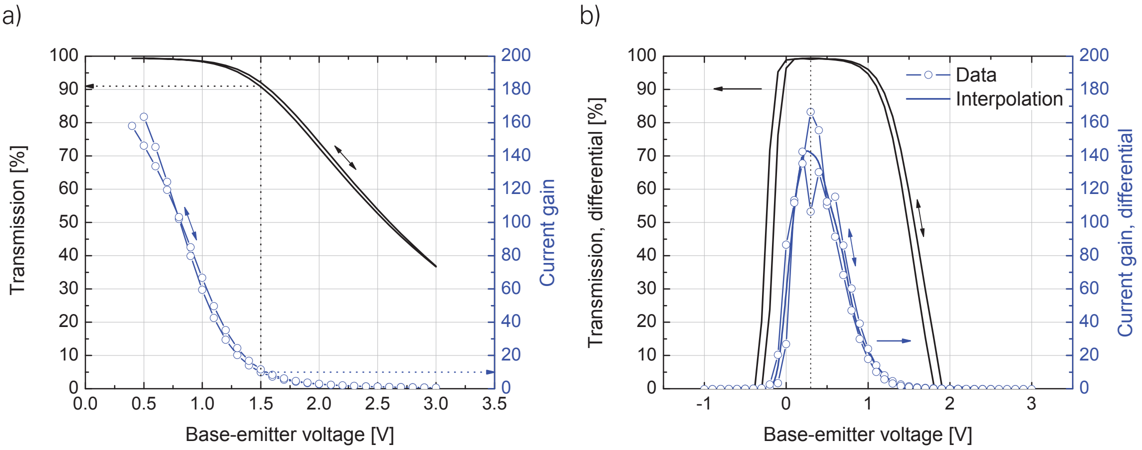

Figure 5.6: Transmission and current gain, calculated for a base sweep measurement with top electrode as emitter in the case of a) absolute, and b) differential magnitudes.

connected by the relation $\beta_{\text{diff}} = \alpha_{\text{diff}}/(1 - \alpha_{\text{diff}})$. The advantage of these values is that they are underestimated whenever currents of the BC diode in backward direction contribute to the overall collector current [182]. Thus, their maximum can be understood as a lower boundary for the maximum possible transmission and current gain achieved by the transistor (s. Sec. 3.3.5). This is further relevant for applications by representing the capability to amplify small current signals. In Fig. 5.6b), the highest transmission obtained is 99.38% corresponding to a differential current gain of ca. 160. In comparison to values calculated by direct transmission, similar values are obtained, but the latter method is more trustworthy. The result is comparable to the work of Nakayama *et al*. who realized an n-type VOT using Me-PTCDI (bottom) and C_{60} (top) as the semiconducting material and achieved a similar current gain [168].

5.5 COMMON-BASE CONNECTION

Measurement The bidirectional operation of the C_{60} triode can as well be seen in the common-base connection where the transmission process can be investigated further. For a constant emitter current I_E, the collector potential sweeps from low to high until the saturation of the collector current is reached. Please note that current saturation is a typical feature of this measurement since the transmitted current is not able to exceed the emitter current, assuming that the current flow of the BC diode is negligible. Therefore, a saturation does not necessarily indicate a current saturation in the output characteristics of the triode as discussed in the next section. In Fig. 5.7a), the top electrode is used as emitter. The collector current saturates at a level close to the injected emitter current, indicating a very high transmission. At the same time, the current of the BC diode in backward direction remains comparatively low. One can determine the respective current flow $I_{BC} = I_C(I_E = 0\,\text{A})$ by setting the current at the emitter to zero. The entire current reaching the collector is then given by charges injected at the base. The fact that the transmitted current for $I_E < 0\,\text{A}$ can be clearly distinguished from the current of the BC diode allows for a proper determination of the transmission. Furthermore, applying a negative collector-base voltage leads to charge injection at the collector, accompanied by a negative collector current. In this range, the transmission is suppressed by the inversely directed electric field between base and collector, and superimposed by electrons injected at the collector. As a consequence, the collector current becomes independent from the emitter current and the curves begin to coincide. The common-base measurement using the bottom electrode as the emitter reveals a similar behavior as previously obtained in the base sweep measurements (cf. Fig. 5.7b)). The transmitted current does not reach the level of the current injected at the emitter, so that the charge carrier transmission seems to be reduced for that operation direction.

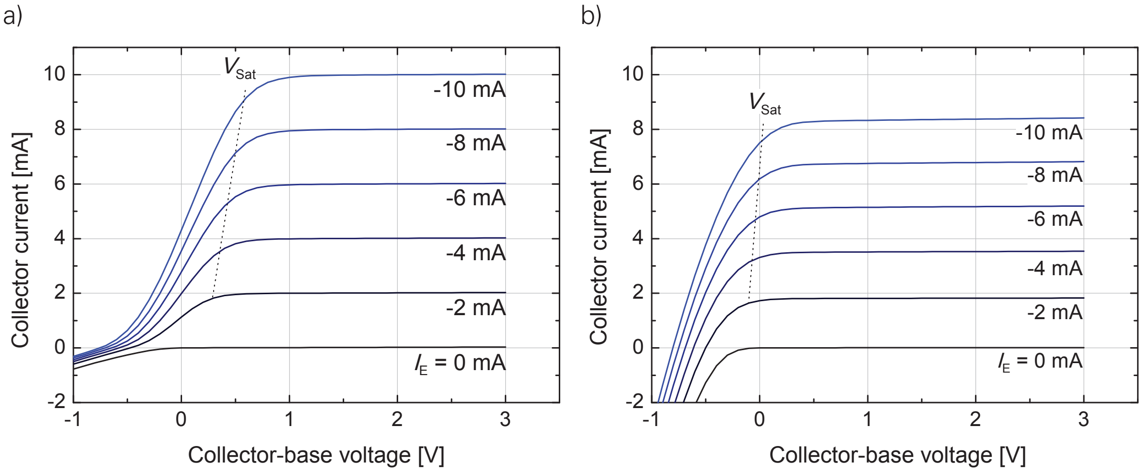

Figure 5.7: Common-base measurement with constant emitter current, revealing the characteristic of the transmission current for a) top electrode as the emitter, and b) bottom electrode as the emitter. The saturation voltage V_{Sat} is indicated by dotted line, shifting approximately linear towards higher base-collector voltages with increasing emitter current.

Transmission characteristic In order to calculate the transmission factor α, one has to compare the transmitted current with the injected current at the emitter:

$$\alpha = -\frac{I_{\mathrm{C}} - I_{\mathrm{C}}(I_{\mathrm{E}} = 0\,\mathrm{A})}{I_{\mathrm{E}}} \quad . \tag{5.7}$$

For vanishing currents of the BC diode in backward direction, the common-base characteristics of the collector current are proportional to the transmission factor, showing that this measurement enables a more direct access to the transmission process. Figure 5.8 exemplarily presents the transmission characteristics, using the top electrode as the emitter. For the top electrode as the emitter, a transmission up to 99.82% can be reached, whereas the highest charge carrier transmission for the bottom electrode as the emitter ranges between 85% and 91%. Thus, the common-base measurement confirms the findings of the base sweep measurements that the operation direction with top emitter and the bottom collector is superior. However, there is a further difference between both transmission directions: The saturation voltage V_{Sat}, determined at the collector-base voltage where the transmission equals 90% of the maximum transmission, is different [182]. For the top electrode as the emitter, the saturation takes place between 0.3 and 0.6 V, depending on the emitter current. For the opposite operation direction, the transmission current saturates at ca. 0.6 V lower collector-base voltages, as it can be seen in Fig. 5.7. This reveals that there are intrinsic device parameter which influence the saturation behavior. In this way, a high charge carrier transmission between 75% and 85% can be already realized at a

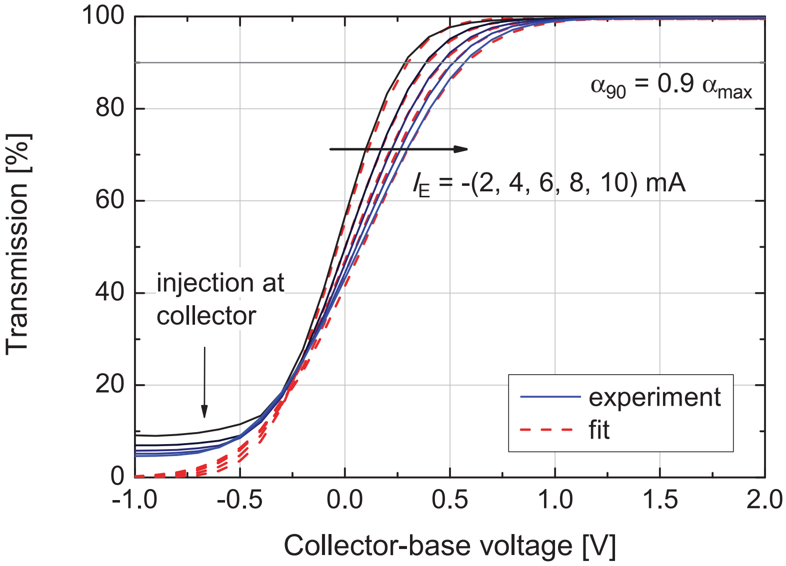

Figure 5.8: Transmission characteristics in common-base connection, using the top electrode as the emitter.

collector-base voltage of 0 V if the bottom electrode is used as the emitter. Similar for both measurements is the shift of the saturation voltage towards higher base-collector voltages with increasing emitter current.

A further optimization of VOTs by reducing this saturation voltage will be essential to reach a very low driving voltage. For that purpose, several strategies are discussed here. First of all, one could do a gedankenexperiment in which the base electrode is perfectly insulated and any current flow involving this electrode is prohibited. Hence, for current injected at the emitter, charge carriers have to leave the device by the collector contact, independent from the collector-base voltage. A variable emitter voltage guarantees that charge carriers will be pushed to the collector. The collector current in a common-base measurement now equals the constant emitter current for all collector-base voltages. Since this is not observed, an insufficient insulation of the base electrode is one reason for the decrease of collector current below the saturation voltage. Furthermore, if the collector-base voltage is negative, charge injection at the collector might arise whose current is superimposed to the transmission current. This fact could also interfere with the charge carrier transmission by redistributing the charge carrier density in the collector layer, so that the transmission factor would be negatively influenced. However, the main reason for a reduced charge transmission is a too low collector-base voltage needed in order to transport charges to the collector, and thus avoiding the development of a space-charge zone on the collector side. Since the internal voltage drop in the BC diode can be increased by a built-in potential, its implementation is one tool to reduce the saturation voltage. This has been demonstrated for pentacene triodes, controlling the built-in voltage by using a doped layer at the collector [491].

Although it is not yet possible to unambiguously assign these possible influences to the measurement, a mathematical description of the transmission behavior can be done. For example, such a description is interesting for a later implementation of triodes into a circuit simulation program where the characteristic transmission behavior has to be reproduced. One way to do this is, based on an empirical analysis, to fit the transmission curves in Fig. 5.8 by a Gauss error function

$$\alpha(V_{\mathrm{CB}}) = \frac{\alpha_{\max}}{\sigma\sqrt{2\pi}} \int_{-\infty}^{V_{\mathrm{CB}}} \exp\left(\frac{(V' - V_0)^2}{2\sigma^2}\right) dV' \tag{5.8}$$

with V_0 and σ the mean location and the standard deviation of the corresponding Gaussian distribution. $\alpha_{\max}$ is the maximum transmission reached at $V_{\mathrm{CB}} \to \infty$. It is found that for all emitter currents, the transmission behavior can be fitted by an error function. Only at negative collector-base voltages, a discrepancy is obtained due to charge injection at the collector electrode. While $\alpha_{\max} = 99.6\%$ is constant for all curves, the median position V_0 increases from -0.05 V to 0.07 V with increasing emitter current. At the same time, also the standard deviation σ increases from 0.12 V to 0.34 V. This results in increasing saturation voltages, so that higher collector-base voltages are necessary to reach high transmission at high emitter currents. As a consequence, on-state conditions with high collector currents are typically accompanied by a decreasing transmission value, as already demonstrated by the base sweep measurement in Sec. 5.3. The main reason might be that for increasing emitter currents the base-emitter voltages increases and thus a growing number of electrons drop into the base electrode, as revealed by the diode characteristics in Sec. 5.2. Besides that, it is obvious that the collector-base voltage has to increase in order to realize a proper conduction of the increasing amount of charge carriers transmitted to the collector if the resistance of the collector layer is assumed to be constant.

Feedback The bidirectional operation of the VOT already supported the assumption of a permeable base electrode. A further indication would be the presence of a feedback from the collector potential onto the emitter. Without any openings in the base electrode, the electric field on the collector side is completely screened from the electric field on the emitter side of the device. Direct connections between the bottom and the top intrinsic layer of the VOT allow for a punch-through of the electric field and thus generates a feedback, similar to a vacuum tube triode. Therefore, a change in collector potential can influence the injection at the emitter contact. This phenomenon has been described first for a vacuum tube triode, defining the feedback as

$$D = -\left.\frac{\partial V_{\mathrm{BE}}}{\partial V_{\mathrm{CE}}}\right|_{I_{\mathrm{C}}=const.} \tag{5.9}$$

comparing the change in the base-emitter voltage V_{BE} with a variation of the driving voltage V_{CE} in order to keep the collector current I_{C} constant. This parameter can be calculated using a common-base measurement due to the constant collector current if the collector-base voltage exceeds the saturation voltage. Fig. 5.9 exemplarily evaluates the feedback for the top electrode as the emitter. Curves shift to the right with increasing absolute emitter current in accordance to the shift of the saturation voltage. In the range of 1 V to 3 V, where the collector current of the corresponding measurement in Fig. 5.7 is constant, the feedback drops from values between 10% and 30% to ca. 5%. For comparison, Spangenberg mentions that the feedback of a vacuum tube triode is typically in the range of 0.5% to 40% [201, p. 206].[3] This demonstrates that although vacuum tube triode have large openings in their grid electrode, VOTs based on C_{60} can reach similar values even with a base electrode without predefined openings. It indicates the existence of non-metallic paths between the emitter and the collector electrode, so that the base

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[3] The feedback is the inverse of the 'amplification factor' given in Ref [201, p. 206].

electrode, consisting of a 15 nm thin Al layer must have regions which do not screen the electric field distribution. Together with the bidirectional operation of the C_{60} triode, it is reasonable to assume that the base electrode has openings, too. A short explanation of the origin of the high feedback values will be given in Sec. 7.4 where an advanced understanding of the distribution of the electric field and the charge carrier distribution will be applied. Below 1 V, the condition $I_C = \text{const.}$ is not fulfilled and the equation

$$g_m * D / g_d = 1 \quad , \tag{5.10}$$

introduced in Sec. 3.3.5, is not valid anymore. Nevertheless, the feedback value still represents how the emitter can be influenced by the collector, and the highest feedback values are obtained in the voltage range between 0 V and 1 V. Here, the feedback has a maximum value in the range of 70% for all curves, shifting from around 0.2 V to 0.5 V for increasing absolute emitter current. This is exactly the voltage range where the saturation voltage of the common-base measurement is located (cf. Fig. 5.8). It indicates that whenever charge carriers injected at the emitter are increasingly collected by the collector, after previously passing the base electrode, a strong interaction between the collector potential and the emitter potential takes place. However, if the modulation of the transmitted current saturates, the effect of the collector potential on the emitter reduces.

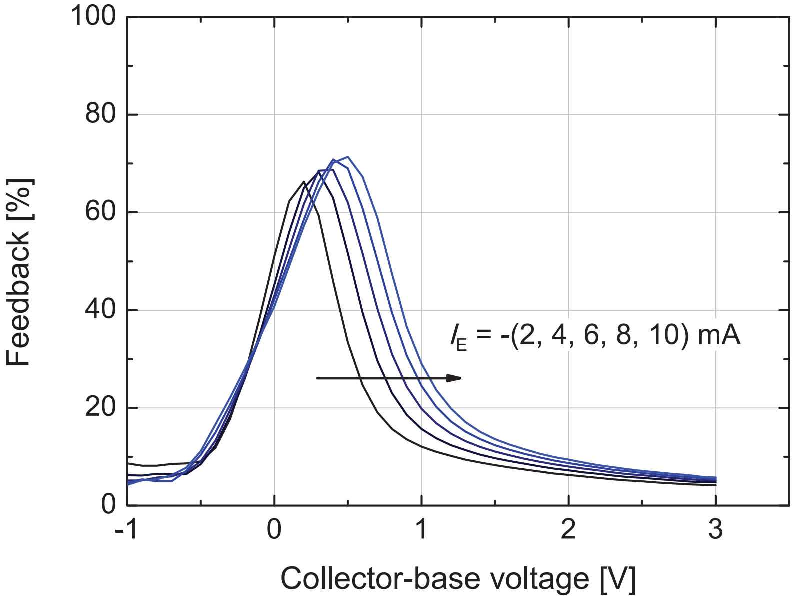

Figure 5.9: Feedback in a common-base connection vs. collector-base voltage using the top electrode as the emitter. In the range from 1 V to 3 V, the collector current shown in Fig. 5.7 is almost constant and values can be evaluated. The feedback is between 10% and 25% at V_{CB} =1 V, depending on the emitter current, and it drops to around 5% at the highest collector-base voltage.

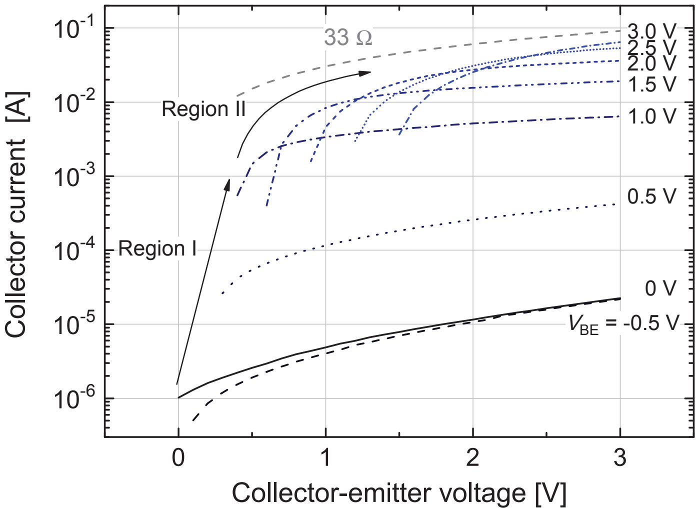

Figure 5.10: Output characteristics of a C_{60} triode using the top electrode as the emitter. The dashed line represents a current flow through a resistor with 33 Ω at the given collector-emitter voltage.

5.6 OUTPUT CHARACTERISTIC

The output characteristic shows the transistor operation at various driving voltages, and is therefore most helpful to determine the behavior of the transistor in a circuit. In a common-emitter configuration, the collector potential V_C is varied from the emitter potential $V_E = 0\,V$ to a maximum driving voltage. This is done for various constant base potentials V_B so that every curve of the measurement represents a unique IV characteristic of the device which is set by the base-emitter voltage. Figure 5.10 presents the output characteristic of a C_{60} triode using the top electrode as the emitter. At $V_{CE} = 3\,V$, the current of each curve increases with the increasing base-emitter voltage, in accordance with the base sweep measurement. Some of the curves do not start at $V_{CE} = 0\,V$, but at higher voltages. The reason is that only positive values of the collector current are shown in this semi-logarithmic plot. Clipped data points correspond to negative collector currents relating to electron injection at the collector.

Essentially, the measurement can be divided into two regions. In the first region, for base-emitter voltages ranging from -0.5 V to 1 V, currents strongly increase with the base potential. This operation mode can be associated with the exponential region of the base sweep measurement in Fig. 5.3a) where the highest subthreshold swing occurs. The behavior in this region is accompanied by only a small shift in voltage for the occurrence of the first positive collector current. It can be seen that for a base-emitter voltage of 1 V, the driving voltage can be reduced below $V_{CE} = 1\,V$ without tremendous loss in collector current. At this operation point, the collector current density would still be around 100 mA/cm^2. The situation changes in the second region. With increasing base-emitter voltage, the occurrence of the first positive collector current strongly shifts to higher voltages. Compared with the base sweep measurement, this is the operation range where the on-state is reached and higher base-emitter voltages eventually lead to a decrease of collector current. This is accompanied by high currents flowing off the base electrode (cf. Fig. 5.3). Especially, if the driving voltage is low ($V_{CE} < 1\,V$) and the base-emitter voltage is high ($V_{BE} > 1\,V$), the base potential is higher than the emitter or the collector potential, so that both outer electrodes of the triode inject charges, flowing towards the base electrode. This right shift of the curves in region II means that a higher driving voltage, e.g. 3 V, is necessary to reach high collector current densities around 1000 mA/cm^2 (ca. 40 mA). To avoid the presence of region II, one has to minimize the leakage current flowing into the base electrode. If this current could be completely suppressed, all curves would have zero collector current exactly at zero driving voltage, similar to an OFET.

Furthermore, the on-state resistance can be evaluated. In Fig. 5.10, the current of a resistance with 33 Ω is plotted vs. the driving voltage which seems to be an upper limit for the device currents. This value corresponds to the inverse of the transconductance $g_\mathrm{m} = 30\,\mathrm{mS}$ determined by the base sweep measurement. Although the on-state resistance R_On of the device and the maximum transconductance do not necessarily coincide, it might be that both parameters are limited by the resistance of the electrodes. This is reasonable since the electrode resistance of the present mask setup has been measured to be in the range of tens of Ohms. Furthermore, as it will be shown in Sec. 8.4, higher on-state current densities can be reached if the influence of the electrode can be decreased by shrinking the active area.

Finally, the saturation of the collector current can be investigated. For a field-effect transistor, it is a common observation that currents saturate and do not depend on the driving voltage anymore. This is different to a C_{60} triode. Figure 5.10 demonstrates that currents increase over the whole range of the collector-emitter voltage, independent of the base-emitter voltage. However, at some base potentials, the curves increase sublinearly if one compares with the dashed line of the resistor. Thus, C_{60} triodes do not show a pronounced saturation regime. Similar observations are found for OFETs with a channel length below 1 µm exhibiting short channel effects [114]. This behavior is directly linked to the feedback. As given by Eq. 5.10, the device resistance and the feedback are indirect proportional. Any change in collector-emitter voltage leads to an influence at the emitter contact. Since the base-emitter voltage is set constant, every rising electric field at the emitter contact implies a larger injection current which gets transmitted through the base electrode and reaches the collector. Therefore, the feedback should be minimized in order to reach a more pronounced current saturation.

5.7 FREQUENCY-DEPENDENT MEASUREMENT

After the device has been characterized in the previous sections, the function of the C_{60} triode is confirmed in a real circuit. Therefore, a voltage amplifier in a common-emitter configuration is realized. The circuit is shown in the inset of Fig. 5.11. The VOT is connected in series to a resistor and a constant supply voltage of $V_\mathrm{dd} = 6\,\mathrm{V}$ is applied. Changing the resistance of the transistor by the base potential leads to a potential shift between the VOT and the resistor inversely proportional to the voltage change at the base electrode. This is why this setup is also called an inverter circuit. At the working point $V_\mathrm{BE} = 0\,\mathrm{V}$, the resistor R is set to a value determining that half of the supply voltage drops over the transistor, allowing for the highest voltage gain. A sine wave with a peak-to-peak voltage of $V_\mathrm{pp} = 100\,\mathrm{mV}$ is applied to the base by a signal generator, and the output is measured by an oscilloscope. In Fig. 5.11a) the voltage gain

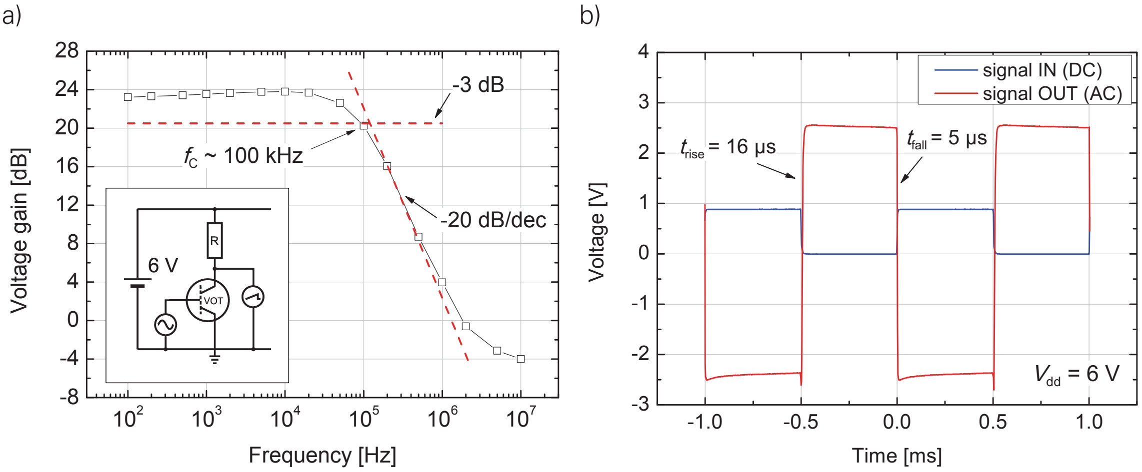

Figure 5.11: a) Frequency dependence of the small signal voltage gain using an inverter circuit with $R \sim 1.7\,\mathrm{k\Omega}$. The gain drops by -3 dB at 100 kHz. The gain-bandwidth product is about 1.5 MHz. The dashed line is a guide to the eye for a decay of -20 dB/decade. b) Pulsed measurements, revealing rise and fall times in accordance to a). The C_{60} triode shows clear switching properties for a pulse repetition frequency of 1 kHz.

of the circuit is shown. The circuit exhibits a clear signal inversion and a maximum voltage gain of 15 at low frequencies and the drop to -3 dB at 100 kHz points to a gain-bandwidth product of 1.5 MHz. Thus, this C_{60} triode exhibits operation close to the HF-regime. The decay of -20 dB/dec, related to a 1/f-dependence of an RC element, indicates that it might be possible to achieve even higher frequencies by reducing capacitances and resistances of the device as well as of the circuit configuration. For example, if one determines the time for charge carriers to move from the emitter to the collector contact assuming a device length of the order of the total intrinsic layer thickness (200 nm), a mobility of 0.1 cm^2/Vs and a voltage of 3 V, a transit time of 1.3 ns is calculated, which would correspond to a maximum switching speed of 120 MHz. Thus, further improvement in time response of the C_{60} triode seems to be possible. For the same inverter circuit as used above, an additional pulsed measurement at a supply voltage of 6 V is performed. The resistor is set to 1 kΩ and the pulses vary the base-emitter voltage between 0 V and 1 V with a repetition rate of 1 kHz. The output signal has a clear inversion and a peak-to-peak voltage of ca. 5 V. Fall and rise times, measured by reaching 90% of the final value, are 16 μs and 5 μs, respectively, in good agreement with the cutoff frequency of 100 kHz determined before. As a consequence, the function of the C_{60} triode is proven in a real circuit and amplification of voltages is realized which is conceivable to be a future application of this device. The fact that a resistor is introduced to the circuit already represents a certain limitation to the transistor under investigation since the driving voltage dropping over the triode changes. For example, the voltage gain-bandwidth product is rather a lower bound of the transistors capability. However, an exact determination of the transistors transit frequency, defined as the frequency where unity current gain is reached, is not possible since the collector and the base current have to be accurately measured at a constant driving voltage, applying a small signal amplitude.

5.8 INTERMEDIATE SUMMARY

In this chapter, general characteristics of C_{60} triodes have been discussed. The device function was proven by a base sweep measurement, showing operation with a current density of 1000 mA/cm^2 at a driving voltage of 3 V. Several parameters, like a subthreshold swing of 200 mV/decade, an on/off ratio greater than 10^3, a high transconductance of 30 mS, and a maximum current gain of 160, could be determined. A special property of these devices is the bidirectional operation. The top as well as the bottom electrode can be used as the emitter, albeit the former gives superior results. Related to this is the feature of the base electrode to allow for a high transmission of charge carriers in both direction, indicating a permeable electrode which enables charge flow through openings directly connecting the upper and the lower i-C_{60} layer. This conclusion is further supported by the high feedback between 5% and 70%. An advantage of the bidirectional operation is the possibility to stack other devices like OLEDs or organic memory devices on top or underneath the triode, increasing the freedom of device integration. Finally, a proof of the device function in an inverter circuit demonstrates that MHz-operation is in reach, realizing a voltage gain-bandwidth product of 1.5 MHz.

6 EFFECT OF ANNEALING

Two process steps turned out to be essential for the preparation of functional transistors: Firstly, the base electrode is exposed to air for 15 min in dark. It is well known that aluminum quickly oxidizes and forms native aluminum oxide AlO_x, saturating in a thickness of a 2-3 nm [463, 465, 492]. This self-passivation arises from the fact that aluminum oxide is impermeable for oxygen or water after a certain oxide thickness is reached (c. Sec. 4.4.3). Secondly, after finishing the fabrication and encapsulation, samples are annealed. Here, it will be shown that this annealing step is essential for the device operation. Various measurement techniques are used to determine the influence of the annealing onto different device properties. If not claimed otherwise, annealing is done for 2 h at a temperature of 150 °C.

6.1 CHARGE CARRIER TRANSMISSION

The main effect of annealing is a huge increase in charge carrier transmission to a value enabling a clear current amplification over the whole operation range. This can be seen in Fig. 6.1a) where a base sweep of a C_{60} triode as introduced in Sec. 5.1 is shown. Right after fabrication, the device has a very low transmission current and the collector current does not exceed 1 mA/cm^2 for any base-emitter voltage. The difference between the current in the on-state and the off-state is less than one order of magnitude. However, after annealing, the on-state current density strongly increases and now reaches values close to 1 A/cm^2, whereas the off-state current density is not changed. Thus, the annealing leads to an improved performance and enables a further characterization of the device. The motivation for the annealing step can be seen in Fig. 6.1b), presenting the maximum differential transmission over the time passed since fabrication. The samples are fabricated without annealing. It is seen that the charge carrier transmission continuously increases over time. After 120 days, a transmission of 80% is reached and the C_{60} triode achieves a current amplification of 4 without any further post-treatment. The devices are stored in the dark, excluding an effect enabled by irradiation of visible light. It is most reasonable to assume that thermally activated processes can modify the device already at room temperature.

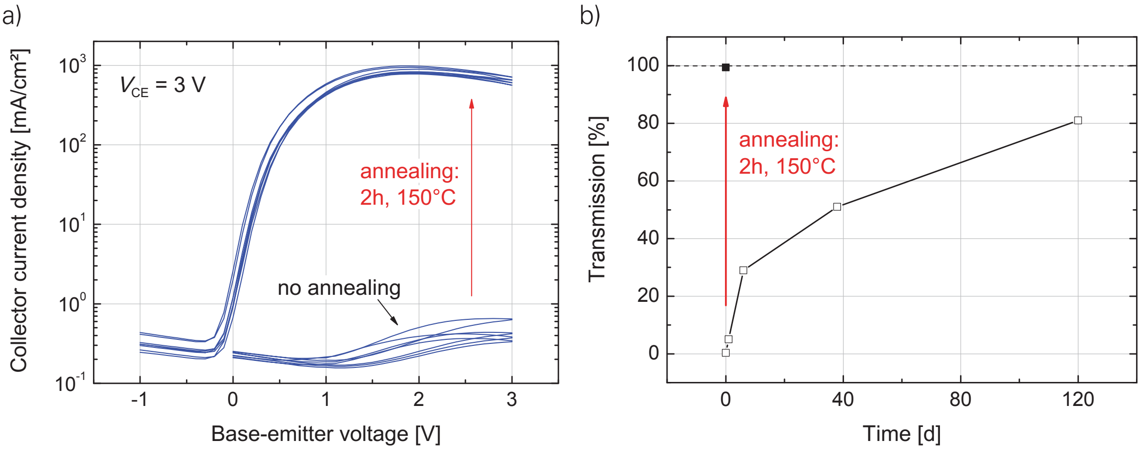

Figure 6.1: a) Base sweep at a driving voltage of 3 V before and after annealing. b) Maximum differential transmission of a C_{60} triode over time passed since preparation. After a storing time of nearly 4 months, the sample reaches a charge carrier transmission of 80%. This process accelerates if the sample is annealed at 150 °C for 2 h, resulting in a subsequent transmission of 99.38%.

From this point of view, it might be helpful to anneal the C_{60} triodes afterwards to initiate and accelerate these positive effects. Indeed, the annealing is able to improve the charge carrier transmission from 0.3% after fabrication to 99.38%, and the collector current increases by three orders of magnitude. Further studies are performed in Sec. 8.5, showing that temperatures of at least 150 °C are required to reach a very high transmission. For lower temperatures, the charge carrier transmission does not reach the maximum. If one considers an industrial fabrication process of such devices, short processing times are important to reach a high throughput. In that sense, annealing is an important step to guarantee a high performance device within a short preparation time. The following sections are intended to examine the processes taking place during annealing.

6.2 SHEET RESISTANCE AND TRANSMITTANCE OF THE BASE ELECTRODE

To measure sheet resistance and transmittance of the base electrode, Al is deposited onto 100 nm C_{60}, ensuring similar growth conditions to those present in the VOT. The setup is presented in Fig. 6.2b). For each thickness *d*, varying between 0 nm and 25 nm, one sample is produced on a glass substrate by thermal vapor deposition and encapsulated in nitrogen atmosphere afterwards. Additional electrodes are evaporated to contact the thin Al layer outside the encapsulation glass. The sample layout equals the setup developed by Schubert *et al.* for calcium degradation tests [493]. Transmission spectra are measured with a spectral photometer Shimadzu UV-3101 and evaluated at 800 nm where C_{60} has the highest transmittance. The sheet resistance is determined by a 4-wire measurement.

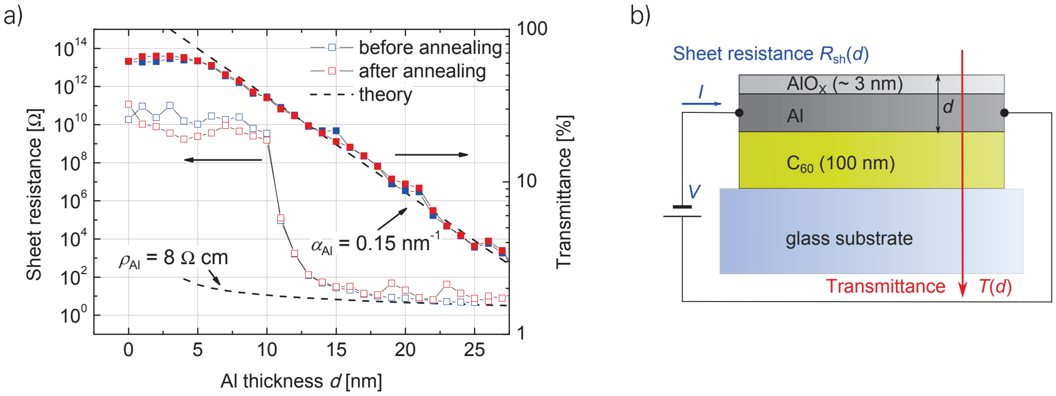

Figure 6.2: a) Sheet resistance and the transmittance of the Al base electrode vs. its thickness. Annealing is done for 2 h at a temperature of 150 °C. For comparison, dashed lines represent theoretical solutions. b) Measurement setup. The sample geometry corresponds to the setup used in Ref. [493].

The transmittance T over Al film thickness d, shown in Fig. 6.2a), has first a plateau up to 5 nm and then follows a typical exponential law as described by Beer's law

$$T(d) = \exp\left(-\alpha(d - \Delta d)\right) \tag{6.1}$$

where α is the absorption coefficient and Δd a constant shift in thickness. A dashed black line overlaid to the transmittance values corresponds to an absorption coefficient of 0.145 nm^{-1}, meaning that approximately every 7 nm, the light intensity will be attenuated by a factor corresponding to the Euler number e. However, this agreement is only reached by shifting the curve to the right using Δd =3 nm. Thus, optically, the Al thin film behaves as if it would be constantly 3 nm thinner, in agreement with a thin aluminum oxide layer which is transparent and does not influence the transmittance. Therefore, the plateau is affected by the transmittance of 100 nm C_{60}, which is constant for all samples. It can be assumed that the Al of samples with a layer thickness of only a few nanometers is completely oxidized. Reaching 4 to 5 nm, Al forms metal cores which are still not connected. Although the oxide layer is schematically shown on top of the Al thin film, it is reasonable to assume that the lower side of the base electrode is at least partially oxidized. The total oxide layer thickness determined in this experiment, however, cannot specify where the aluminum oxide forms. The percolation threshold, i.e. the film thickness where the metal grains become interconnected, can be electrically determined by measuring the sheet resistance of the Al thin film (cf. Fig. 6.2). At 10 nm or less, the metallic layer has such a high resistance that the measured currents are limited by the resolution of the source-measuring unit. The sheet resistance drastically drops when the thickness exceeds 11 nm and first conductive paths appear along the layer. For the electrode thickness used in the VOT as base, 15 nm, a sheet resistance of 30 Ω/sq. is obtained. This value is in the range of a thin indium-tin-oxide layer used as a transparent but conductive electrode for OLEDs [494]. For comparison, the sheet resistance

$$R_{sh}(d) = \rho_{Al}/(d - \Delta d) \tag{6.2}$$

is plotted in Fig. 6.2a) with ρ_{Al} as the specific resistance of the Al layer. Fitting yields a specific resistance of 8 µΩcm, three times higher than for bulk aluminum which might arise from the polycrystalline structure of the metallic layer [495]. As for the optical transmittance, an Al thickness reduced by a Δd of 3 nm accounts for the insulating properties of the aluminum oxide.

For the device performance of the VOT, changes of the Al film arising from the annealing step play a key role. Therefore, all samples are remeasured at room temperature after 2 h at 150 °C on a hot plate in a nitrogen atmosphere. No significant changes appear, neither for the transmittance nor for the sheet resistance. As a consequence, it can be assumed that the oxide layer does not grow any further, which is expected to shift the transmittance values as well as the percolation threshold of the electrical conductivity to higher Al layer thicknesses. Thus, the thin metal layer is still intact and can be used as a conductive electrode in the VOT. Moreover, morphological changes of the Al thin film after annealing discussed in the next section have no significant effect on the conductivity of the electrode.

6.3 INVESTIGATION OF MORPHOLOGICAL CHANGES

Due to the weak van-der-Waals bonding between adjacent molecules in the organic solid, even rather small temperature increases can already enable morphological changes. Materials which tend to form crystals usually grow in polycrystalline layers. The size of the crystals can be varied either by using different substrate temperatures or by a post process annealing step [356, 404]. For that reason, it seems likely that C_{60} thin films undergo similar changes during annealing.

X-ray measurements of C_{60} thin films In order to investigate morphological changes within the intrinsic C_{60} layer, X-ray diffraction measurements are carried out, using a grazing-incidence angle (GIXRD). The method is advantageous: Since the organic thin films have a thickness of only 50 to 100 nm, the amount of irradiated medium is strongly increased by keeping the incident angle small. As Elschner *et al.* argue, X-rays do not penetrate the substrate due to total reflection at the interface between the material to be investigated and the glass substrate [496]. Furthermore, X-ray reflection (XRR) measurements are done to investigate variations of the layer thickness and roughness. In this experiment, 100 nm C_{60} are deposited onto a glass substrate by thermal vapor deposition in vacuum. The measurement is performed under ambient conditions and repeated after annealing[1]. Figure 6.3a) shows the result of the GIXRD measurement at an incident angle of 0.2° after subtraction of the background measured at an incident angle of 0.1° where no diffraction by C_{60} is visible. The presence of peaks clearly reveals the presence of C_{60} crystallites in the thin film. The pattern, normalized to the highest peak, is in agreement with Ref. [496] and does not show any substantial changes after annealing. Stetzer at al. [343] as well as Vogel [497] also did not observe morphological changes or decomposition of C_{60} at the applied temperature. Thus, neither the height ratio between the peaks nor the width of the peaks changes, and it can be concluded that the size of the C_{60} crystallites remains unchanged after annealing. A different result from that would indicate that annealing is able to change the molecular arrangement in the C_{60} thin film and as a consequence the device geometry of the C_{60} triode. Using the Scherrer

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[1] Measurement is done by Dr. Lutz Wilde from Fraunhofer CNT, Dresden using a Bruker D8 Discover diffractometer. Details are similar to Ref. [496]

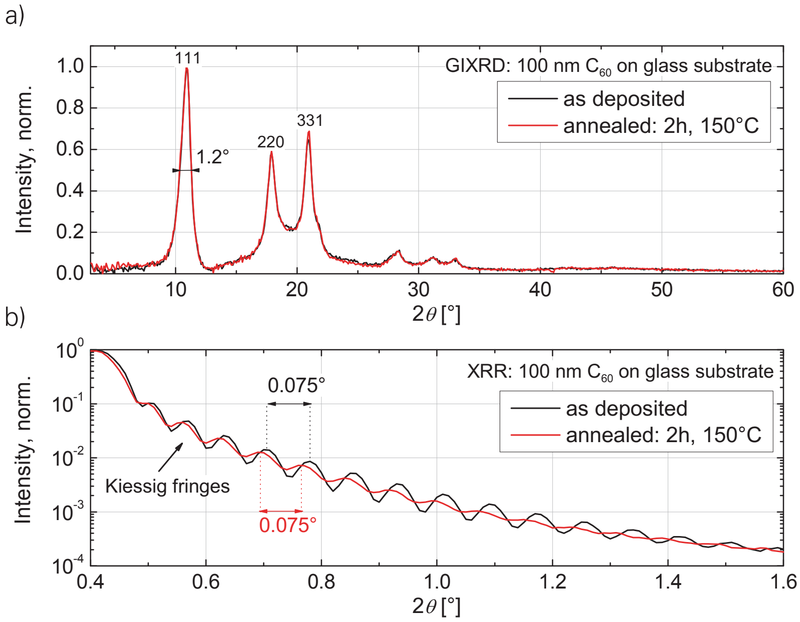

Figure 6.3: a) GIXRD measurement of 100 nm C_{60} on glass substrate before and after annealing. The incident angle is 0.2° b) XRR measurement of 100 nm C_{60} on glass substrate before and after annealing.

equation

$$D_{\mathrm{hkl}} = K\lambda/(B_{\mathrm{hkl}}\cos(\theta))\,, \tag{6.3}$$

the mean crystallite size can be estimated [498]. $K \approx 0.9$ is a geometry factor, B_{hkl} the width of the peak at the half maximum in radians, θ the Bragg angle, and λ the wavelength of the radiation. An evaluation for the (111)-peak located at $2\theta = 10.95°$ with $B_{111} = 1.2°$ yields a crystallite size of around 7 nm, in agreement with Ref [499] for C_{60} on SiO_2. Since the method delivers the most precise results for crystallites with diameters well below 100 nm, the estimated value is trustworthy. A C_{60} layer as used in the VOT is therefore composed of several small C_{60} grains.

Further information about the effect of annealing on the C_{60} thin film is presented in Fig. 6.3b), showing XRR measurements. There, the intensity of the reflected beam is measured while varying the incident angle. Whenever Bragg's law is fulfilled by the total thickness of the investigated layer and the incident angle, the signal strength is enhanced. Due to the high order resonances, the peaks are repeated at higher angles. As a result, Kiessig fringes emerge which can be used to determine the density of the material together with the layer thickness, and their slope and decay depends on the roughness of the layer [500]. Simulations are done to qualitatively reproduce the XRR measurement, shown in the Appendix section A.2, and the result of the fit will be discussed here. First of all, the layer thickness can be accurately determined to be 104 nm before and 105 nm after annealing, revealing a 5% error with respect to the targeted value. The density of the materials remains unchanged, 1.68 g/cm^3, in accordance with Ref. [329] and [501]. A determination of the roughness leads to erroneous results since the slope of the curve is not fully matched by the simulation, pointing to the fact that the simulation accounting only for a glass substrate and a C_{60} layer may not be sufficient to reproduce the experimental data. Nevertheless, as seen in Fig. 6.3b), the Kiessig fringes are weaker for the annealed sample at higher angles, which indicate an increase in layer roughness. For example, the simulation gives a roughness (rms) of 2.5 nm before and 3.5 nm after annealing, having a similar decay as observed in the experiment

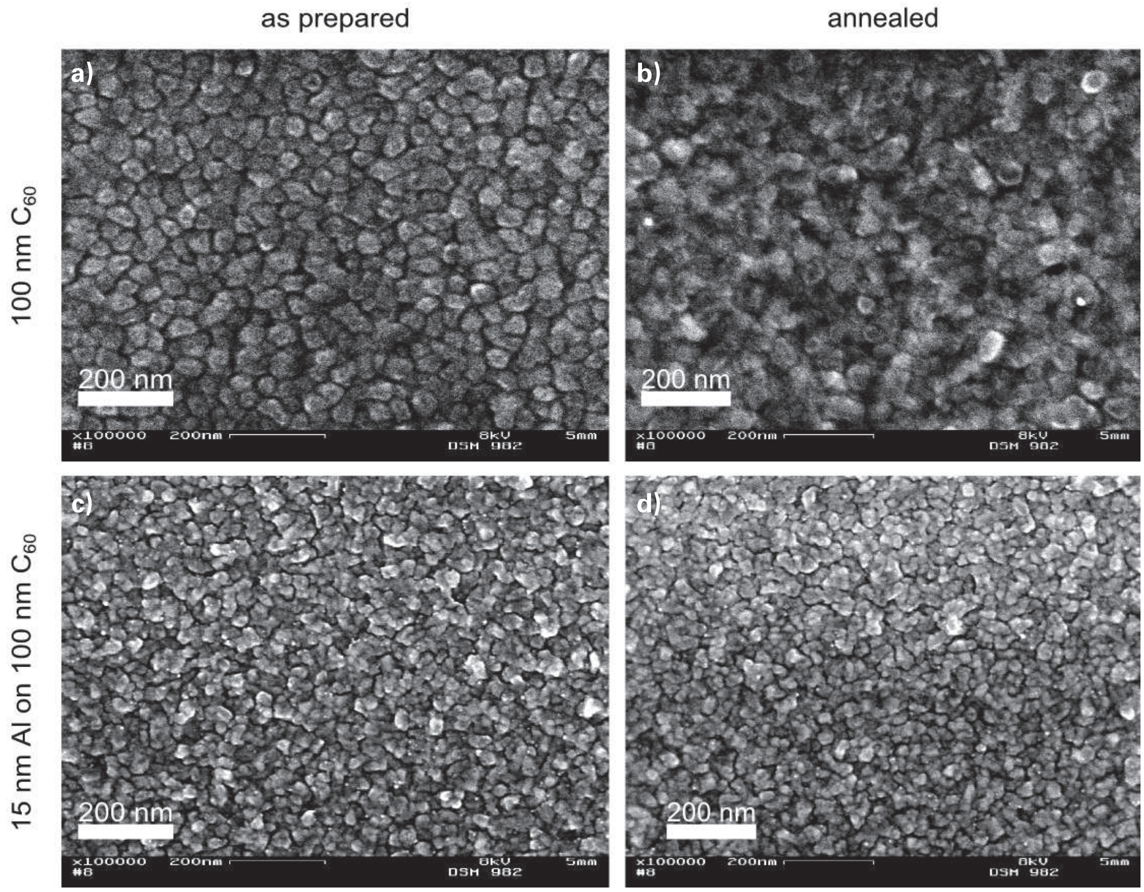

Figure 6.4: SEM pictures of a) 100 nm C_{60} on Au/Al b) 100 nm C_{60} after annealing c) 15 nm Al on 100 nm C_{60} on Au/Al d) 15 nm Al on 100 nm C_{60} after annealing. a) and b) represents the structure of the bottom C_{60} layer, whereas c) and d) represent the base contact.

for each processing step. In summary, the C_{60} layer seems to be stable against annealing and does not change its thickness, density, or crystallite structure, but it cannot be excluded that morphological changes at the surface of the layer take place. As a reason, it should be mentioned that C_{60} molecules embedded in the layer have more neighboring molecules than molecules located at the surface, so that their intermolecular binding energy via attractive dispersion forces is increased.

SEM measurements To visualize morphological changes, scanning electron microscopy (SEM) measurements are carried out on the surface of the C_{60} layer or of a thin Al layer deposited onto this C_{60} layer. The sample setup equals the bottom diode of the C_{60} triode, i.e. the sample consists of a glass substrate with a bottom electrode of 50 nm Al and 20 nm Au, followed by 100 nm of C_{60}. A section of the sample is finally covered by 15 nm Al, representing the base electrode, and the entire sample is exposed to air for 15 min. After breaking the sample into two parts, one of them is annealed at 2 h at 150 °C on a hot plate in a nitrogen atmosphere. Thus, all samples are composed by the same layers, making the experiments highly comparable. To load the sample into the SEM, they are exposed to air, but the measurement itself is carried out at high vacuum conditions. A DSM 982 Gemini SEM (Zeiss) is used with an acceleration voltage of 8 kV and a magnification of 100000x. SEM measurements of all four combinations, with and without an Al layer on top as well as before and after annealing, are performed[2].

Figure 6.4a) shows the typical morphology of a C_{60} thin film. The features of the grainy structure are in the range between 25 nm to 50 nm, likely to be composed of several C_{60} crystallites with a size of about 7 nm estimated by the GIXRD measurements. The appearance of the surface seems to be homogeneous over a wide range, and no contamination is observed on the surface. This finding is corroborated by AFM measurements shown in the Appendix A.3. After annealing, the C_{60} surface changes, and it is hardly possible to locate the single features observed before annealing. Most features seem to be blurred and intermixed with their neighbors, and several edges become more pronounced. Thus, this imaging method reveals a similar result as obtained by the XRR measurements, showing a certain increase in layer roughness and a surface modification after annealing.

Next, Al layers grown on C_{60} films are investigated. Fig. 6.4c) and d) present the results before and after annealing, respectively. The Al layer exhibits a structure which is regularly interrupted by deep grooves, having a distance which is in the range of the size of the C_{60} grains. This fact suggests that the covering of Al is influenced by the underlying structure of the C_{60} thin film. In principle, these grooves can be interpreted as parts where Al is missing, thus building potential openings for charge carrier transmission. However, the SEM image could as well be explained by deeper lying parts, emitting electrons in a less efficient way with respect to metal features located higher or having sharper edges. Nevertheless, it can be concluded that the thin film growth of Al on C_{60} does not lead to a uniform coverage which could inhibit a possible pinhole formation. However, the existence of openings in the Al layer can be proven unambiguously.

After annealing, the appearance does not change significantly. It can be stated that the SEM measurement is not able to resolve any morphological changes of the Al layer, induced by the annealing. The same sample setup is used to perform atomic force microscopy (AFM) and the result is presented in the Appendix section A.3. There, similar results are obtained. Within an imaging area of 1 µm × 1 µm, no significant changes of the Al surface are observed and the layer roughness slightly changes from 2.17 nm to 2.34 nm. The AFM measurement cannot give substantial hints for pinhole formation, but it also does not exclude pinholes since the information obtained by the topography is not able to distinguish between a pinhole and the Al layer. Both methods, SEM and AFM, give an impression of the surface characteristics of the base electrode, but they do not resolve the layer thickness of the Al layer which is directly related to pinholes.

TEM measurements A more detailed characterization of the base electrode can be made by using transmission electron microscopy. This technique allows to measure the thickness of the layers under investigation but requires the transmission of electrons through the sample. This is enabled by a high electron energy and by keeping the sample as thin as possible, typically in the range of 100 nm. For that reason, instead of a glass substrate, a copper grid holding a 20 nm carbon layer is used which can be easily transmitted by electrons. Layers to be investigated are deposited on this substrate by thermal vapor deposition. A 50 nm C_{60} layer followed by a 15 nm thin Al layer is used to simulate the growth of the base electrode onto the bottom C_{60} layer.

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[2] Measurements are performed together with Susanne Goldberg, Institut für Physikalische Chemie, TU Dresden

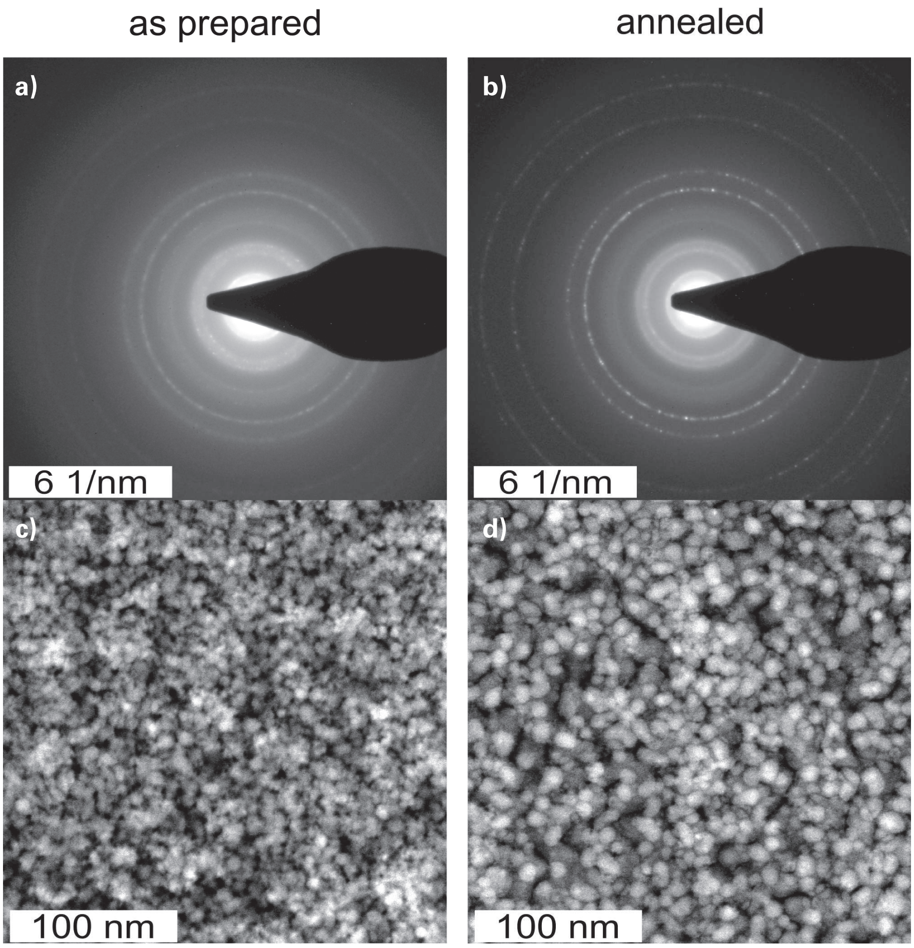

Figure 6.5: Transmission electron microscopy of 15 nm Al deposited on 50 nm C_{60}. The substrate for the thin film deposition consists of a 20 nm thin carbon substrate held by a copper grid. a) Diffraction pattern and c) scanning TEM (STEM) measurement of a sample as prepared. b) and d) Corresponding measurement for a sample after annealing. The STEM measurement images the thickness of the Al layer and by using the dark field mode, thick regions appear bright whereas dark regions point to thinner layer thickness. A qualitative change after annealing is observed. The Al grains get larger and more concentrated. As a consequence, it is reasonable to assume that regions in between the Al grains become thinner and eventually form an opening in the Al layer. The diffraction patterns a) and b) confirm the result. They show stronger and sharper reflexes after annealing, especially for the Al 111- and 220-peak (c. Fig. 6.6). Furthermore, single reflexes appear, indicating that single crystals contribute. This result points to the formation of larger and better ordered Al crystallites within the polycrystalline layer.

Samples are exposed to air for 15 min before some of them are annealed. Measurements are done using a TEM Tecnai F30 (manufacturer: FEI) and an electron energy of 300 keV [3].

Figure 6.5 presents the result for a sample before and after annealing for two different measurement techniques. The diffraction pattern (a) as well as a scanning TEM (STEM) picture using the high-angle annular dark field detector (c) are shown for a sample as prepared. They can be compared to measurements of an annealed sampled in (b) and (d). Since both samples are fabricated at the same time, they only differ in the annealing step, increasing the comparability and the reliability of the measurement. While the STEM is running, the area is scanned by a focused electron beam. The transmitted and scattered electrons are detected whereas the directly transmitted beam is ignored. Materials with a higher atomic number Z appear brighter since the interaction with electrons is enlarged. Moreover, for thin samples as used here, the scattering intensity and thus the brightness of the image linearly depends on the layer thickness. The C_{60} layer is relatively smooth and the atomic number of carbon ($Z = 6$) is less than half of the one for aluminum ($Z = 13$) so that mainly the aluminum thin film will contribute to the measured intensity. This is further supported in appendix section A.4 by a comparison of picture brightness and the emitted X-ray intensity of Al.

In contrast to the SEM images shown above, the TEM images show a smaller segment of the sample. However, if one compares structures within a similar scale before annealing, it is found that the STEM measurement reveals a finer granulation of the Al thin film with features in the range of 5 to 10 nm, whereas the features of the SEM measurement have dimensions in the range of 20 to 50 nm. It can be assumed that these grains correspond to Al crystals (c. appendix section A.4). However, these Al grains agglomerate in clusters, appearing as brighter regions on average, with a distance between each other similar to the feature size found in the SEM images of Al on C_{60}.

To understand the difference between both imaging methods, SEM and TEM, it should be mentioned that TEM displays the thickness of the layer whereas SEM rather shows the surface of the layer. Considering that in a SEM measurement, individual features at the top side of the base electrode appear relatively flat, it is likely that the fine granulation revealed by the STEM measurement is due to the bottom side of Al layer. This is reasonable because the formation of an interface between a metal and an organic layer depends on their deposition sequence. I.e. whether the metal is evaporated onto a molecular layer or the molecules are deposited onto the metallic layer [502]. In the first case, metal atoms are able to penetrate into the organic layer due to their smaller size and the weak van-der-Waals bonding of the organic solid. Furthermore, evaporated metal atoms have a high kinetic energy if they impinge on the molecular layer, and as a consequence, an interdiffusion layer is formed where both layers mix [73, 503, 504]. In the second case, molecules reaching a metal surface or an oxide surface are unable to penetrate into the layer underneath. Thus, the bottom and the top surface of the Al layer, acting as the base electrode, are supposed to be qualitatively different.

After annealing, the TEM picture reveals a morphological change of the Al layer towards larger Al grains. Now, the thin film seems to consists of fewer but larger Al grains. This is again confirmed by conventional TEM measurements presented in the appendix section A.4. Simultaneously, the

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[3] Measurement done together with Dr. Thomas Gemming, IfW Dresden

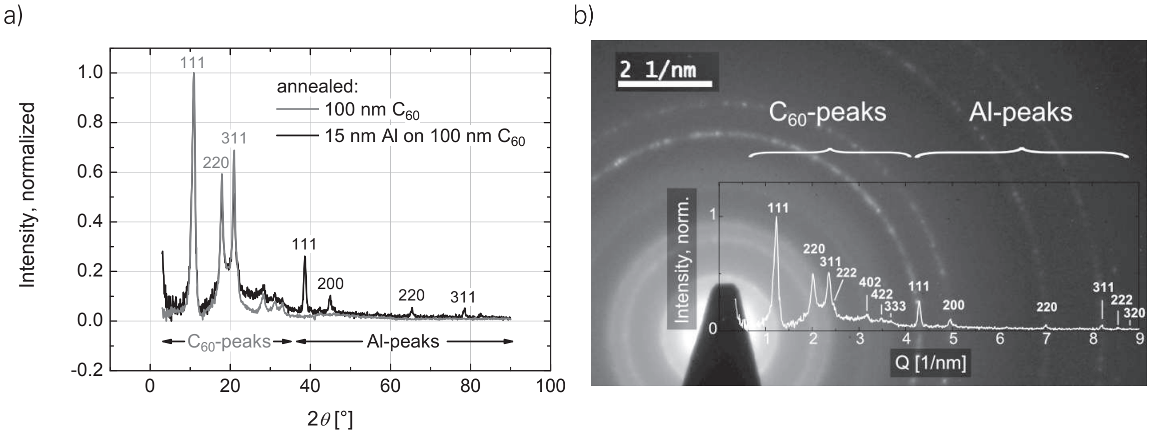

Figure 6.6: a) GIXRD measurement of a sample with 100 nm C_{60} on glass substrate compared to a sample with additional 15 nm Al. First peaks are corresponding to the fcc structure of C_{60} with a lattice constant of 14.1 Å. Above 35°, no further peak of the C_{60} layer is visible and thus all peaks arising there for the Al covered sample can be attributed to this metal. Again, a cubic lattice can be revealed with a lattice constant of ca. 0.4 nm. b) Comparison of the GIXRD measurement of an Al covered sample (annealed) with a diffraction pattern obtained by a transmission electron microscope. If the angle 2θ is converted into wavenumbers, rings of the diffraction pattern are in excellent agreement with the peaks. While the rings generated by C_{60} are relatively homogeneous distributed, Al rings show contributions from single reflections of Al crystallites.

SEM picture of the annealed Al layer does not show a significant change. For that reason, it is expected that most of the variations take place at the bottom side of the Al layer where due to the probable interdiffusion of Al into the C_{60} layer, the electrode is less defined. The fact that individual Al crystallites are coalesced by the annealing step can be further seen by the diffraction pattern obtained for a circular area (diameter: ca. 1 µm). Figure 6.5a) and b) present the measurement done with the electron microscope for a sample as prepared and after annealing. There are several rings visible which indicate on the one hand the presence of regular structures, but on the other hand the presence of a polycrystalline thin film. Furthermore, the rings are not fully uniform, showing in part enhanced reflexes from small single crystallites within the detection area. Since C_{60} as well as Al tend to form crystallites, a further analysis requires the assignment of the rings.

To identify the rings of the diffraction pattern and to assign them to either Al or C_{60}, GIXRD measurements are compared in Fig. 6.6. The pattern of an annealed 100 nm C_{60} thin film shows the typical strong peaks 110, 220, and 311 as already discussed in literature for a face-centered cubic cell of the C_{60} lattice [323, 496]. If now a 15 nm thin film of Al is added to the layer stack, emerging peaks can be assigned to Al. Indeed, above $2\theta = 35°$ peaks appear, indicated as 111, 200, 220, 311, in agreement with Bragg's law for a lattice constant of 0.4 nm for Al [505]. Thus, the difference between the lattice constants of C_{60} and Al enables a clear distinction between their diffraction patterns. With that knowledge, the rings of the diffraction pattern can be assigned by a comparison of the GIXRD measurement and the diffraction pattern obtained with the electron microscope in Fig. 6.6. The magnitude of the scattering vector

$$Q = \frac{2\sin(\theta)}{\lambda} \tag{6.4}$$

is calculated to match the x-scale of both measurements. Then, the peaks of the GIXRD measurement and the rings of the diffraction pattern match: the inner rather blurred rings are from the C_{60} layer, whereas the outer rings, appearing somewhat sharper, are assigned to the Al layer on top.

Now, the diffraction patterns in Fig. 6.5 can be compared. The annealing leads to a sharpening of the Al peaks, so that the blurring between the rings decreases. Thus, the size and the uniformity of Al crystals are increased by annealing. At the same time, the C_{60} layer remains unchanged by the annealing. The enhanced crystallization of the Al layer has a strong implication for the understanding of annealing for C_{60} triodes. All processes taking place evolve towards thermodynamic equilibrium and minimize the Gibbs free energy G of the system [506]. Furthermore, after evaporation of the Al, there are many centers where grains start to grow, so that different crystal orientations meet at the grain boundaries where the Gibbs energy of the thin film is enhanced due to non-ideal stoichiometry and interatomic distances. The recrystallization of neighboring grains finally leads to the coalescence of individual grains and the lowering of the Gibbs free energy. As a consequence, there are central points attracting material, and regions from which material leaves. Then, it might be possible that openings are formed in the layer which directly link the upper and the lower C_{60} layer in case of a C_{60} triode. If for the change in Gibbs energy $\Delta G < 0$ is fulfilled, this process will run spontaneously, but accelerates at higher temperatures. This would explain why the charge carrier transmission already increases at room temperature, but if the sample is annealed at elevated temperature, it reaches a value close to 100%, as argued in Sec. 6.1. The fact that exactly the same annealing step as used for the C_{60} triode leads to a reorganization of the base is a strong hint that the morphological changes induce the improved charge carrier transmission of the VOT.

In order to study the pinhole distribution, shape, and size, an STEM image with a modified brightness scale is presented in Fig. 6.7. The resolution of the picture is 0.26 nm per pixel. Pixels with zero brightness, corresponding to potential pinholes are highlighted by enhancing the brightness of all other pixels. The correction is carried out in a way that the underlying thin film structure is still visible. Pinholes are arranged between the clusters of Al grains and it becomes obvious that their shape is not necessarily circular. Elongated structures can exceed a length of 10 nm, but anyhow they seem to be interrupted and not continuously connected. The typical minimum diameter of the pinholes starts with the size of a single pixel and ranges up to about 5 nm. Larger pinholes occur rather rarely. Here, it should be noted that pinholes with a diameter smaller than the size of the C_{60} molecule are not able to be filled by the organic semiconductor, so that depending on the cross-section of the pinhole, large intermolecular distances exists, hampering the charge transport. Thus, openings actively contributing to the transmission current should have a minimum diameter of ca. 1 nm. In order to estimate the fraction of the area the pinholes occupy, the darkest pixels are counted and compared with the total pixel number. The resulting amount of only 0.45% demonstrates that openings are rather small and far apart from each other. Even if pixels with 5% of the maximum brightness are taken into account, their area does not exceed 1%. The mean distance between neighboring pinholes is estimated to be in the range between 10 nm and 50 nm. An exact value is difficult to calculate since it is unknown which of the pinholes actively contribute to the transmission process.

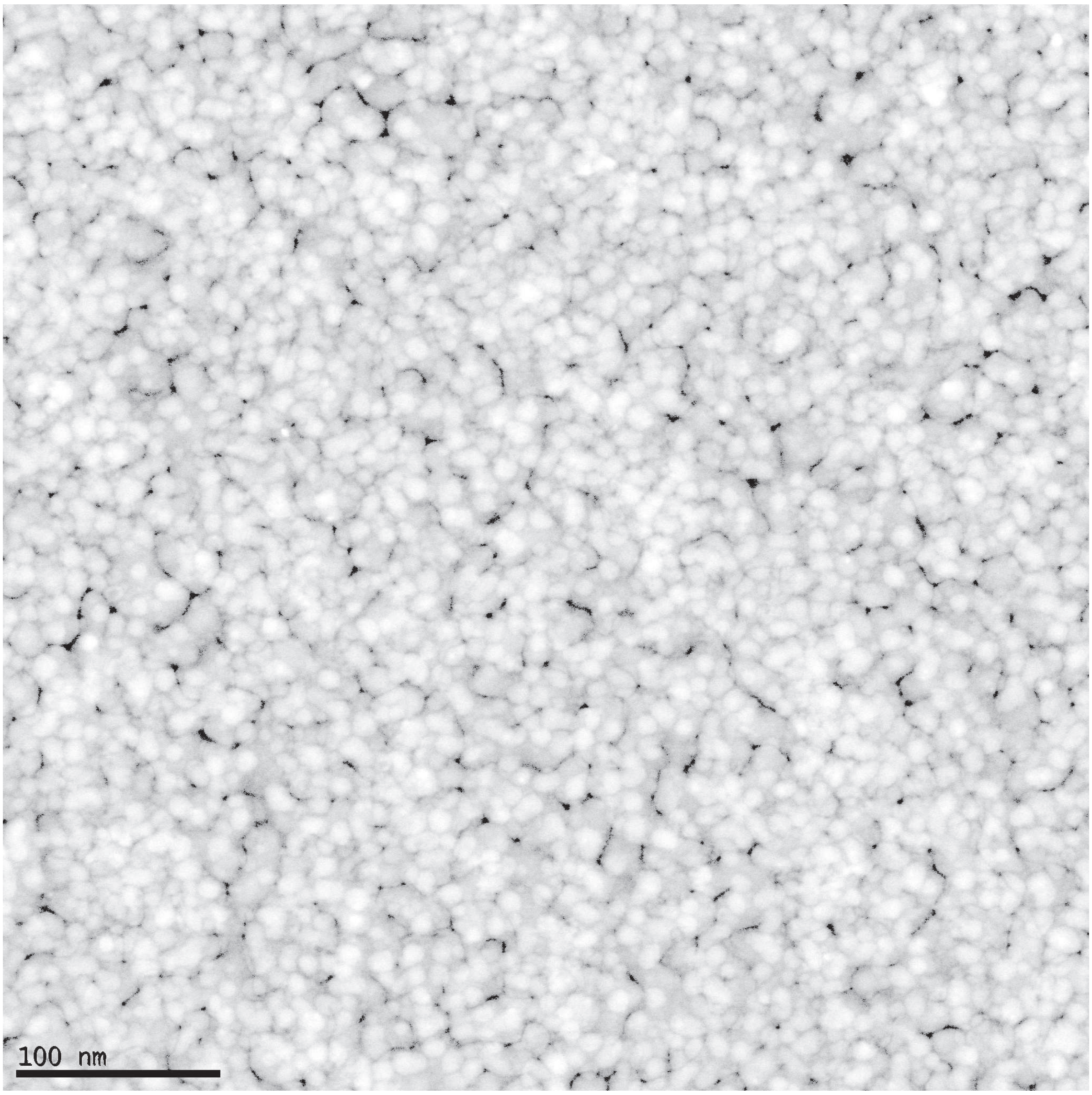

Figure 6.7: STEM image of 15 nm Al deposited on 50 nm C_{60} after annealing, with modified brightness scale. Pixels with zero brightness are unchanged whereas all other pixels are lightened up. Thus, the distribution of potential pinholes in the base electrons becomes visible.

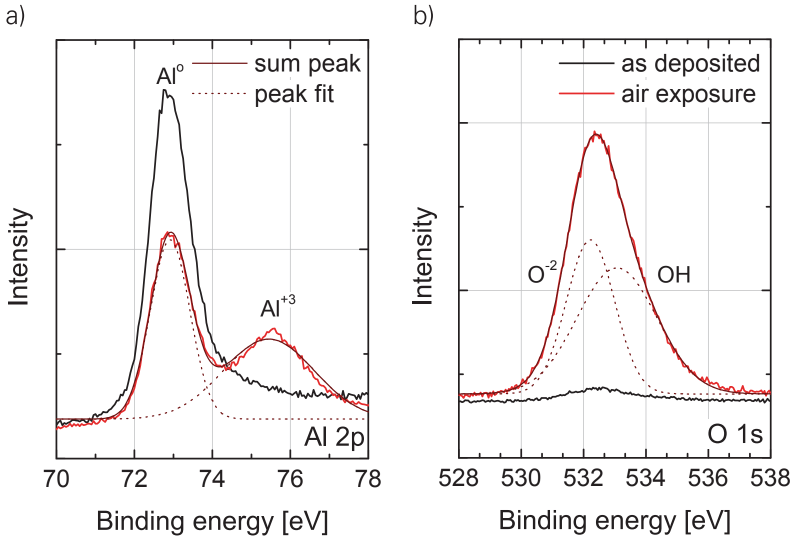

Figure 6.8: XPS measurement of an Al thin film as deposited and after air exposure, showing a) the Al 2p peak and b) the O 1s peak. Before air exposure, a low amount of oxygen is present and one Al peak is found, corresponding to an Al-Al binding. After air exposure, the amount of oxygen increases and an additional Al 2p peak appears, representing a binding between Al and O.

6.4 PHOTOELECTRON SPECTROSCOPY OF THE BASE ELECTRODE

Ultraviolet photoelectron spectroscopy (UPS) and X-ray photoelectron spectroscopy (XPS) are used in order to investigate the effect of annealing on the energy alignment at the interfaces of the base electrode and on the formation of the aluminum oxide [4]. Further details about the measurement setup and the method can be found in Ref. [53] and in the Experimental section 4.3.4.

The upper interface of the base electrode For the top diode, the upper surface of the base electrode is relevant. A sample setup is designed, which represents the upper half of the layer sequence of the C_{60} triode. First, on a glass substrate, 50 nm Al are deposited, representing the base electrode. Then, the sample is exposed to air (ca. 3 min) to grow an aluminum oxide layer. The third step is the evaporation of 10 nm C_{60} onto the oxidized Al layer which corresponds to the top C_{60} layer of the C_{60} triode. Finally, the sample is annealed. After each of these steps, UPS and XPS measurements are performed. Figure 6.8a) presents the XPS signal of the Al 2p peak. Right after deposition of the Al, a single peak at the position of 72.9 eV appears, indicating neutral aluminum (Al^0) as it occurs in pure Al [465, 507]. If there would be a substantial amount of oxidized aluminum on the surface of the sample, an Al^{+3} peak at lower binding energies should appear. Indeed, at 75.4 eV a slightly enhanced signal is visible, pointing to a small amount of oxygen in the sample which can be explained by gettering residual oxygen and water from the vacuum chamber. This is supported by Fig. 6.9b) where the intensity remains quite small at the position of the O 1s peak [465].

The situation changes after the sample is exposed to air. Now, the amount of oxygen strongly increases, accompanied by an increase of the Al^{+3} peak and a decrease of the Al^0 peak. A native

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[4] Measurements are performed together with Max L. Tietze (IAPP) and Martin Schwarze (IAPP), using a Phoibos 100 system (Specs, Germany) at a base pressure of 1×10^{-10} mbar.

oxide layer forms on the surface of the Al layer and the fact that the Al^0 peak remains still visible reveals the presence of pure Al underneath the oxidized layer. Thus, the native oxide is only a few nanometer thick because the electron inelastic mean free path in metals is about 3-4 nm [508]. The ratio between the two Al 2p peaks, I_m and I_o for the contribution from the metal and the oxide layer, respectively, gives more information about the exact thickness d_ox of the oxide layer [509]. The corresponding equation derived by Strohmeier [507]

$$d_\mathrm{ox} = \lambda_\mathrm{m} \sin\left(\theta_\mathrm{TOA}\right) \ln\left[\frac{N_\mathrm{m}\lambda_\mathrm{m}}{N_\mathrm{o}\lambda_\mathrm{o}}\frac{I_\mathrm{o}}{I_\mathrm{m}} + 1\right] \tag{6.5}$$

uses the inelastic mean free path of the electrons in the metal $\lambda_\mathrm{m} = 2.58$ nm and in the oxide $\lambda_\mathrm{o} = 2.68$ nm as used by Frerichs *et al.* [492]. Besides that, the atomic densities of metal atoms, $N_\mathrm{m} = 4.61 \times 10^{22}$ atoms cm^{-3}, for the pure and $N_\mathrm{o} = 6.02 \times 10^{22}$ atoms cm^{-3} for the aluminum oxide layer contribute [465, 492]. The take-off-angle θ_TOA measured between the direction of emitted and detected electrons and the sample surface is 90°. A fit of the Al 2p peak with two Gaussian distributions determines the ratio $I_\mathrm{o}/I_\mathrm{m}$ to be 1.03, taken as the area under the curve with respect to the background. Hence, the derived thickness of the native aluminum oxide is about 1.7 nm and thus slightly smaller than given in literature where values between 2 and 3.5 nm are reported [462, 463, 465, 492, 507, 510]. However, the oxide thickness depends on various parameters like purity of the Al, exposure time, and relative humidity of the air. For example, oxidation with dry oxygen results in the lowest oxide thicknesses, ranging from 0.5 nm to 1.4 nm in dependence on the pressure [454, 460].

The O 1s peak gives further information about the composition of the oxide. Aluminum can oxidize via oxygen or water and forms different types of oxide stoichiometry. While the reaction with oxygen leads to Al_2O_3, water is known to incorporate hydroxides into the oxide layer by formation of $Al(OH)_3$ [449]. In Fig. 6.8b), the peak is significantly broadened at higher binding energies, revealing a contribution from oxygen bound with hydrogen, besides the peak due to O^{-2} [465]. These two types of chemical oxygen bonds relate to two different types of oxides formed during air exposure. For example, the two times negative oxygen O^{-2} is typically bound with the three times positive aluminum Al^{+3} to Al_2O_3. Fitting the O 1s peak with two Gaussian signals reveals a ratio between both species of $I_\mathrm{OH}/I_\mathrm{O} = 1.35$. Usually, this ratio is below 1 and from a larger value, one can assume that the native oxide layer consists merely of $Al(OH)_3$ [465]. As a consequence, one has to assume that the oxidation is mainly driven by water. It is also known that aluminum oxide and aluminum hydroxide are converted in one another by releasing or capturing water, depending on the partial pressure [460]. However, the time the sample stays in vacuum between the air exposure and the measurement is not sufficient to rebuild it to aluminum oxide. Due to the unknown stoichiometry of the layer, the native oxide will be referred here as AlO_x even though there is a substantial incorporation of hydrogen.

After proving the formation of a native aluminum oxide by air exposure, its effect on the interface to the top C_{60} layer is investigated. Therefore, the UPS signal is evaluated after each processing step and Fig. 6.9 shows the result. Directly after deposition of the Al layer, the high binding energy cutoff (HBEC) is at 17.19 eV and the work function of the metal lies around 4.03 eV close to the reference value of 4.2 eV [511, 512]. However, the air exposure leads to a clear downshift of the HBEC towards 17.99 eV, resulting in a work function lowered to 3.23 eV. Similar results are obtained in literature and are explained by chemisorbed oxygen and adsorbed water which can

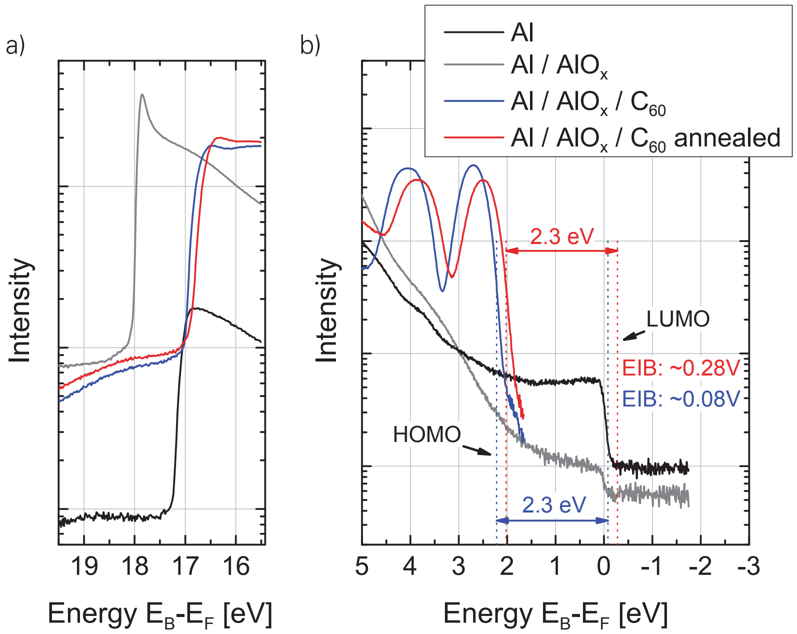

Figure 6.9: UPS measurements at various stages of sample preparation investigate the interface of the base electrode to the upper C_{60} layer. First, the Al as deposited is measured which is subsequently remeasured after air exposure. Further spectra are taken after deposition of 10 nm C_{60} and after an annealing step.

introduce a strong dipole [511, 513–515]. The formation of the oxide layer itself seems to have a small effect on the work function [513]. However, it seems to lower the amount of emitted electrons. At energies around the Fermi level, the fresh Al layer shows a clear edge in accordance with Fermi-Dirac statistics. After the air exposure, this Fermi edge is still visible, but the intensity of the signal decreases due to the native oxide layer.

In comparison to the LUMO level of nominally intrinsic C_{60} at approx. 4.0 eV, such a low work function means that if no charge exchange happened between the oxidized Al and C_{60}, the electron injection barrier would be negative. The UPS measurement demonstrates that this is not the case after the deposition of 10 nm C_{60}. The HBEC shifts back to 16.96 eV and in turn the work function increases to 4.26 eV. It can be assumed that there is a charge transfer from the oxidized aluminum to the C_{60} in order to reach a common Fermi level, eventually counteracting the dipole accompanying the AlO_x layer. Nevertheless, the low work function of the oxidized Al probably causes the nearly vanishing electron injection barrier (EIB) of 0.08 eV using the measured position of the HOMO 2.22 eV below the Fermi level and an energy gap of 2.3 eV determined elsewhere [375, 516]. The EIB increases to 0.28 eV after annealing and the HBEC shifts towards the vacuum level by 0.15 eV resulting in an increased work function. However, if one assumes that the work function of the Al layer is unaffected by the annealing, this variation points to a change of the dipole formation between the aluminum oxide and the C_{60} layer. The reason cannot determined by this measurement, but it might be that adsorbed water is removed from the surface of the AlO_x layer. It can be summarized that the air exposure leads to the well known formation of a ca. 2 nm thin native oxide layer on the surface of the freshly deposited Al layer. The thickness of the AlO_x layer seems to be unchanged by annealing, but the small electron injection barrier increases by 0.2 eV.

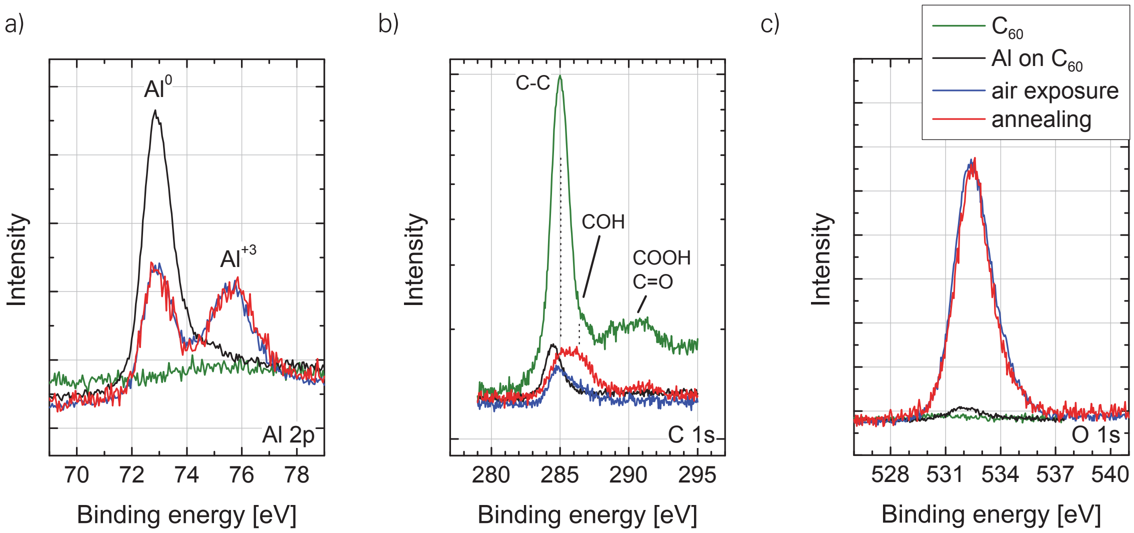

Figure 6.10: XPS measurement of 15 nm Al deposited on 50 nm C_{60}, representing the base electrode. Subsequently, the sample is exposed to air and annealed. Signals are taken for the energies of the a) Al 2p, b) C 1s, and c) O 1s core levels.

The lower interface of the base electrode In contrast to the previous section, an inverse layer structure is employed to investigate the lower interface of the base electrode. Now, the growth of the aluminum on the C_{60} layer similar to the base electrode is studied. Owens *et al*. published related results and were able to show by UPS and XPS measurements that Al is growing rather in island mode than layer by layer [503]. They use a similar substrate temperature of 300 K and a similar layer thickness of Al. Furthermore, they mention that Al atoms diffuse into the C_{60} layer where they occupy interstitial sites and potentially have a dilute doping effect. From that point of view, the island growth could be indispensable to guarantee that spatial variations in the layer thickness appear. However, the formation of pinholes in the base electrode of the C_{60} triode, allowing for charge carrier transmission, seems to be rather caused by the annealing step because samples without annealing do not have a pronounced function.

The layers are grown on a gold substrate, starting with 50 nm of C_{60} corresponding to the bottom C_{60} layer of the C_{60} triode. Then, a 15 nm Al layer is deposited, representing the base electrode. The sample is exposed to air for 1 min and finally annealed in vacuum at 140 °C for 1.5 h until no further change in the XPS spectra is obtained. After each step, UPS and XPS measurements are performed. Figure 6.10 shows the XPS measurement. First, the C 1s peak is discussed. The single C_{60} layer has its highest peak for the bonding between carbon atoms which can be attributed to the C_{60} [517]. At slightly higher binding energies, further contributions related to a carbon binding to hydroxides and oxygen appear, although the O 1s peak reveals no significant contribution from an oxygen bond to carbon. The layer is not exposed to air, so that these signals may arise from residual trace gases in the vacuum adsorbed on the surface of the C_{60} layer. Especially, the pressure within the evaporation chamber (1×10^{-8} mbar) is higher than in the UPS/XPS measurement chamber. After deposition of the 15 nm thin Al layer, the intensity of the C 1s peak decreases but remains clearly visible. Owens *et al*. argue that the remaining carbon signal can be explained by an island growth of the Al because thinner parts of the metal electrode enable X-rays to pass through and interact with carbon atoms of the C_{60} layer [503]. If there would be an Al layer with homogeneous thickness of 15 nm, the intensity should be reduced by more than three orders of magnitude due to the short inelastic mean free path of the electrons.

In the next step, air exposure of the sample leads to a further slight decrease of the C 1s signal. Again, the formation of the aluminum oxide surface layer is clearly visible in Fig. 6.10a) by simultaneous reduction of the Al^0 and rise of the Al^{+3} peak. It is known that aluminum oxide has a ca. 1.5 times higher volume than the original Al incorporated so that a volume expansion of the base electrode seems reasonable [518]. For example, if on both sides of the Al layer an oxide layer of 2 nm exists, the total thickness of the base electrode including the oxide increases by 1.3 nm due to air exposure. Especially, for very thin regions of the base electrode where most of the C 1s signal can originate, this increase means a larger relative change and thus the air exposure can explain the further reduction of the carbon peak. Of course, an equalization of the Al layer thickness due to air exposure would lead to a similar result, but seems to be unlikely as revealed by the STEM measurements.

As shown above, the Al 2p peak ratio can be used to calculate the thickness of the aluminum oxide layer. However, in this case, the requirements are not fulfilled since the oxide forms most likely on both sides of the base electrode facing to the top and to the bottom electrode. Evidence for that is given by the bidirectional operation of the C_{60} triodes as demonstrated in Sec. 5 and an investigation concerning charge accumulation at the oxide layer, presented in the upcoming Sec. 7. Then, the Al^{+3} peak can be enhanced by the second oxide layer underneath the base electrode. Indeed, the two Al 2p peaks now exhibit nearly identical height in comparison to the XPS measurement investigating the upper interface of the base electrode. To reach an oxidation below the Al layer, oxygen or water must have come to this interface. A diffusion through the Al layer is unlikely since the aluminum oxide natively stops in its growth and would eventually lead to an increased electrode resistance which has not been revealed at the beginning of this section. Oxygen does readily diffuse into C_{60} thin films and occupy interstitial sites within the fcc lattice as discussed in several studies [411, 519–521]. However, Eloi *et al.* found that exposure of a C_{60} thin film for 1 h to 1 atmosphere of O_2 in the dark leads to an only 20 nm thin oxygen enriched layer [522]. Although a diffusion in lateral direction beginning at the electrode edges has to be expected, such a diffusion length is too short to reach a proper oxide formation at a central position of the electrode. For that reason, it is likely that even before air exposure happens, pinholes exists in the Al layer, enabling oxygen and water to diffuse into the lower C_{60} layer to realize the lower oxide layer of the base electrode.

As a last step, the sample is annealed in the UHV chamber at 140 °C and simultaneously the XPS spectra are taken. After a time of 1.5 h, no further changes are observed, and the final measurement is taken as presented in Fig. 6.10. The Al 2p peaks remain unchanged and consequently the oxide layer thickness also stays constant. A similar picture is presented by the O 1s peak. The amount of oxygen remains at a high level in comparison to the freshly evaporated Al layer, and no further oxygen take-up is observed. Only the C 1s peak increases and broadens after annealing. The shape of the peak further indicates the presence of two overlapping peaks. While the peak around 285 eV is assigned exclusively to carbon binding, the second peak ($\sim$ 286.5 eV) might emerge from a COH binding as indicated by dotted lines in the diagram. At this point, it is not clear why the latter appears. One explanation might be that C_{60} binds to OH groups incorporated at the surface of the AlO_xlayer. For instance, the air exposure has already led to a formation

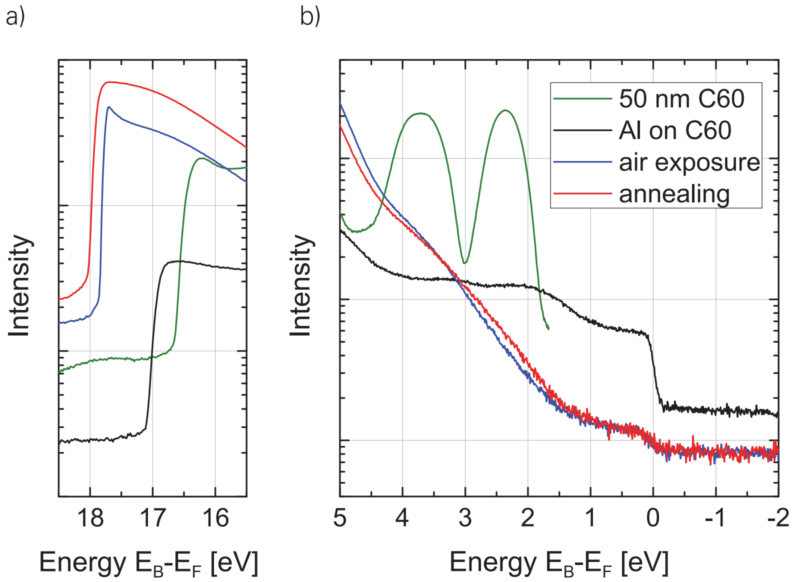

Figure 6.11: UPS measurement of 15 nm Al deposited on 50 nm C_{60}, representing the base electrode. Subsequently, the sample is exposed to air and annealed.

of a shoulder at this energy which is not observed for the measurement of the freshly evaporated Al layer. Nevertheless, the overall increase in C 1s peak intensity points to a morphological change of the base electrode which results in an enhanced variation of layer thickness. Thus, thinner regions become even thinner, and thicker regions grow further. This is in accordance with the TEM measurements, showing that the Al crystallite size increases. From that point of view, the XPS measurement confirms the finding that pinholes form in the base electrode during annealing.

The corresponding UPS measurements are shown in Fig. 6.11. In this measurement, it is not possible to calculate the electron or hole injection barrier since the correct position of the ionization potential in the C_{60} layer is inaccessible after the Al layer is deposited on top. Indeed, the ionization potential of the intrinsic C_{60} layer can be determined prior to deposition of Al, but the interface dipole between the C_{60} and the Al layer remains unknown. Nevertheless, the data can be used in order to analyze the work function of the Al layer regarding air exposure and annealing.

Starting with the C_{60} layer, the Fermi level is found to be 4.55 eV, and the ionization potential, associated with the HOMO onset, is around 6.43 eV with respect to the vacuum level. Thus, the electron affinity, associated with the LUMO onset, lies around 4.1 eV, depending on the energy gap assumed and the Fermi level does not have a mid gap position, but is already shifted to the LUMO level in accordance with literature [331, 375, 376]. The deposition of the Al layer shifts the Fermi level towards 4.11 eV and it has to be assumed that a charge transfer from the metal to the C_{60} layer occurs. After air exposure, a similar effect as previously described happens. The adsorption of water and hydroxide groups on the surface of the AlO_x layer reduces the measured work function to 3.35 eV. Thus, the question remains whether this work function applies also at the lower interface of the base electrode where the adsorption of air components might be hindered due to the direct contact between C_{60} and Al. This fact further complicates the determination of an energy level alignment between the base electrode towards the lower C_{60} layer. However, the work function of the Al layer seems to be low even before air exposure, so that the electron injection barrier possibly vanishes or has a value that does not lead to a pronounced Schottky-barrier. Then, currents injected from the base electrode might only be hampered by the insulating properties of the oxide layer surrounding the base electrode. The formation of the oxide layer is again proven by a clear reduction of the signal intensity around the Fermi edge. Hence, the annealing does not induce further changes. It is interesting that the annealing, able to remove adsorbed water from the surface, does even increase the work function of the oxidized Al layer by 0.18 eV to 3.17 eV, and thus potentially influences the energy alignment.

To shortly summarize, photoelectron spectroscopy reveals the formation of a native oxide layer around the Al electrode with a thickness of 2 nm or less. A subsequent annealing does not change the oxide layer thickness, if the heat treatment is applied in vacuum or in a nitrogen atmosphere but is able to initiate morphological changes in the electrode which point to an increased thickness variation in the Al layer favoring pinhole formation. Furthermore, the low work function of the Al layer, representing the base electrode, indicates a small or vanishing electron injection barrier remaining below 0.28 eV in the case of the upper surface of the electrode in accordance with the literature [379].

6.5 INFLUENCE OF AIR EXPOSURE AND ANNEALING ONTO THE DOPANTS

Dopant degradation In every semiconductor device, interfaces between the metal electrodes and the semiconducting material play an important role. Generally, the energy barriers for charge transfer are non-negligible, leading to a contact resistance. The common tool to overcome this limitation is a highly doped semiconductor region near the metal contact. For electron conducting C_{60} thin films, the tungsten paddlewheel $W_2(hpp)_4$ molecule is a highly efficient electron donor due to its low ionization potential [380, 435, 523]. However, these n-type dopants are difficult to handle in ambient conditions.

If electrons in the ground state of the molecule are located in orbitals with an energy very close to the vacuum level, a chemical reaction with oxygen becomes likely. This oxidation leads to an irreversible modification of the molecule and the compound does not act as an electron donor anymore.

Figure 6.12 shows a conductivity measurement of a 50 nm thin C_{60} film deposited on a glass substrate [5], co-evaporated with $W_2(hpp)_4$ at a concentration of 10 mol%. The conductivity of the thin film is about $5\,\mathrm{Scm}^{-1}$ in agreement with values published elsewhere [380]. Assuming a reasonable electron mobility of 0.1 to $1\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$ for the C_{60} thin film, the charge carrier concentration must be at least in the range of $10^{19}\,\mathrm{cm}^{-3}$ to $10^{20}\,\mathrm{cm}^{-3}$ in order to reach the measured conductivity. This is approximately one hundred to one tenth of the amount of C_{60} molecules per volume. In comparison with the $W_2(hpp)_4$ donor concentration of 10 mol%, a doping efficiency of at least 10% is calculated. Assuming smaller mobilities would require an even higher concentration of free charge carriers. After exposure to air, similar to that used in the VOT fabrication, the conductivity drops by more than five orders of magnitude within 15 min. One might expect that

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[5] Measurement done in cooperation with Novaled AG and kindly provided by them.

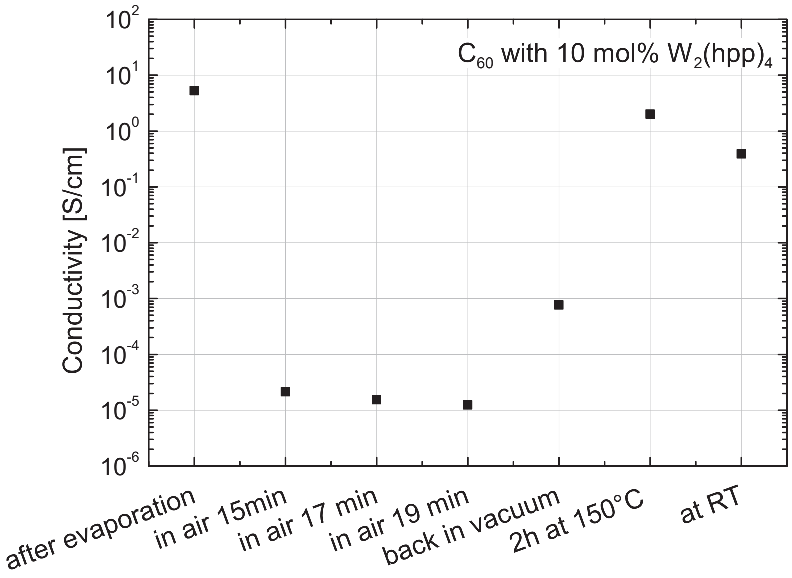

Figure 6.12: Conductivity test of a 50 nm thin C_{60} film doped with $W_2(hpp)_4$ (10 mol%). After fabrication, a high conductivity of ca. 5 Scm^{-1} is measured. Due to exposure to air, the conductivity drastically drops by more than five orders of magnitude. However, by annealing at 150 °C for 2 h, about one tenth of the initial conductivity is restored. This demonstrates that free charges carriers are present in the sample generated by still intact dopant molecules.

this is due to a fast degradation of the dopant molecules. However, after returning the sample to high vacuum conditions, the conductivity rises again and saturates around 10^{-3} Scm^{-1}. Finally, a subsequent annealing step, as used for the VOT increases the conductivity to a value 10 times lower than the initial value. Because of the initially high amount of free charge carriers, it can be estimated that a charge carrier concentration 10^{18} cm^{-3} is still present in the layer, large enough to ensure an Ohmic contact if located near a metal electrode. As a consequence, the strong drop caused by the air exposure cannot be explained by the degradation of the dopant molecules, but rather has to be related to a decrease of charge carrier mobility, initialized by forming traps when oxygen binds to the C_{60} molecules [384, 421, 524–526]. These trap states can further lead to a capture of free charge carriers which also negatively influence the conductivity. Tietze *et al.* studied this effect in more detail, and the results are briefly summarized here [52]. The dopant molecule is passivated in the C_{60} matrix, probably due to the charge transfer from $W_2(hpp)_4$ to C_{60}. Then, energy levels of the dopant are energetically shifted downwards, and a reaction with oxygen becomes more unlikely. In this work, it is shown that after air exposure intact $W_2(hpp)_4$ molecules exist, releasing charges already before annealing is performed. As a consequence, the effect of the increase in conductivity after annealing can be mainly attributed to the increase of charge carrier mobility in C_{60} by removal of trap states, as already mentioned elsewhere in literature [387].

Dopant diffusion The annealing of the samples is an important step to realize high transmission, attributed to the formation of openings within the base electrode. Further, the conductivity of the n-doped C_{60} layer is restored. It remains an open question whether the annealing has some unwanted influence on the doping profile. This can be caused by the low glass transition

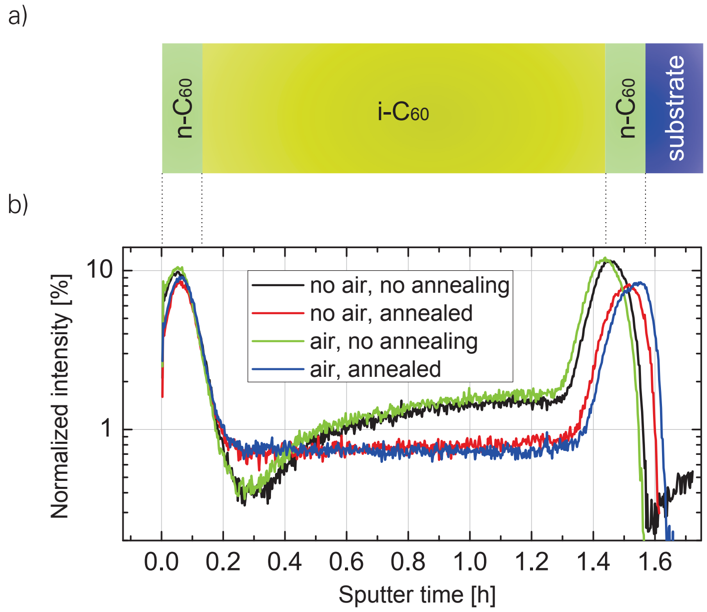

Figure 6.13: TOF-SIMS measurement of an nin-C_{60} layer sequence. a) Schematic layer stack with thickness proportions equal to 20 nm / 200 nm / 20 nm. b) CN profiles for samples exposed to air or not, as well as samples annealed or not.

temperature of most organic molecular layers due to the weak van-der-Waals bonding between the molecules. In the VOT, doped layers ensure an Ohmic injection from the outer electrodes into the device. However, the C_{60} layer close to the base electrode has to remain intrinsic in order to achieve an injection barrier, so that each diode, top or bottom, is able to rectify signals. A dopant diffusion from the doped regions into the intrinsic regions could lead to a decrease of the rectifying behavior of the diodes by decreasing the electron injection barrier between the base electrode and the i-C_{60} layer. For that reason, symmetric devices in a configuration of n-doped (20 nm) / intrinsic (200 nm) / n-doped (20 nm) (nin) layers are prepared on glass substrate and investigated by time-of-flight secondary ion mass spectrometry (TOF-SIMS) depth profiling[6]. In this measurement, the surface of the sample is removed by sputtering layer by layer, and the removed material is analyzed by a mass spectrometer. Details about the method and of a similar measurement can be found elsewhere [527, 528]. Due to the sputtering process, the molecules investigated are decomposed into fragments with stronger covalent bonds between their atoms.

The most significant fragment is a compound of a carbon and a nitrogen atom (CN), as it is present in the hpp ligands of the dopant $W_2(hpp)_4$. Since degradation of $W_2(hpp)_4$ mainly results in formation of $W(hpp)_2$ + O and single hpp ligands, a CN signal corresponds to intact molecules as well as to degradation products [52]. Figure 6.13b) shows the CN profiles of different devices, partly exposed to air for 15 min, and partly annealed for 2 h at 150 °C. The CN intensity was normalized against the total ion intensity in order to remove possible instrument effects, i.e. the intensity axis shows the CN intensity relative to the total ion intensity in percent.

The profile corresponds to the layer sequence as depicted in Fig. 6.13a), showing CN peaks at the beginning and at the end of the sputtering process. Since the profiles reveal similar decays for the CN concentration into the intrinsic region, independent from the sequence of doped and

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[6] Samples are prepared at the IAPP and investigated at the Risø National Laboratory for Sustainable Energy (Technical University of Denmark) by Kion Norrman who has done the evaluation of the data.

intrinsic layer with the sputtering direction, it can be excluded that the doping profile is significantly changed by the measurement. The broadening of the peaks themselves is rather given by the resolution of the TOF-SIMS profiling than by the roughness of the individual layers.

If there would be a molecular diffusion induced by air exposure or by annealing, the height of the CN peaks should decrease, and the entire profile should become more homogeneous. However, the general profile does not significantly change by annealing or air exposure. Assuming that the $W_2(hpp)_4$ is still intact in the untreated sample as supported by the conductivity measurements presented above, a strong diffusion of $W_2(hpp)_4$ after heating the sample, exposed or unexposed, can be excluded. Likewise, the main decay product $W(hpp)_2$ + O seems to show no significant variation since this would also result in a more pronounced change of the CN profile.

However, there is a certain contribution of CN from the intrinsic region which is asymmetric before annealing and which becomes more symmetric afterwards. This means that there must be a further decay product which diffuses into the intrinsic region, mainly starting from the bottom n-C_{60} layer. The heating step is able to enhance the diffusion of this compound, so that the CN profile in the intrinsic regions flattens. Tietze *et al.* showed that after annealing the amount of nitrogen and carbon decreases, but at the same time the amount of tungsten remains constant [52]. From this finding it can be concluded that $W_2(hpp)_4$ or $W(hpp)_2$ + O are not volatile, as opposed to a different decay product of $W_2(hpp)_4$, containing no tungsten. The most probable compound is the hpp ligand which has of course a much smaller size than the original $W_2(hpp)_4$ and thus should rather tend to diffuse through the i-C_{60} layer. Surprisingly, the CN is already present in the intrinsic region before the exposure to air. It might be that some of the $W_2(hpp)_4$ either decomposes after evaporation, or while gettering residual oxygen of the vacuum as well as in the nitrogen atmosphere of the encapsulation. Then, a further exposure to air is not able to generate a higher amount of the corresponding decay product, which is most likely hpp. Since $W_2(hpp)_4$ does not diffuse and other compounds presumably do not generate free charge carriers in a C_{60} thin film, a change in the doping profile by a redistribution of dopants is excluded. Nevertheless, the diffusion of decay products might lead to an enhanced distribution of traps within the i-C_{60} layer.

6.6 ELECTRICAL CHARACTERISTICS OF THE DIODES

CV characteristic of the top diode The role of the aluminum oxide as well as the dopant diffusion can be studied by capacitance-voltage (CV) measurements. For that reason, the top diode of the C_{60} triode as processed in Sec. 5 is investigated. The intrinsic layer has a thickness of 100 nm and the 20 nm doped C_{60} layer has a doping concentration of 1 wt%. Since the C_{60} triode is exposed to air only after fabrication of the base electrode, the upper C_{60} layer has not been in contact with air. Thus, the molecular diffusion of the dopant $W_2(hpp)_4$ can be studied best.

Figure 6.14 shows the measurement before and after annealing for various frequencies, ranging from 1 kHz to 1 MHz. The observed characteristics will be discussed in detail in section 7, explaining the operation mechanism of these transistor devices in terms of Metal-oxide-semiconductor (MOS) diodes. Here, the behavior will be shortly outlined. In backward direction, the applied

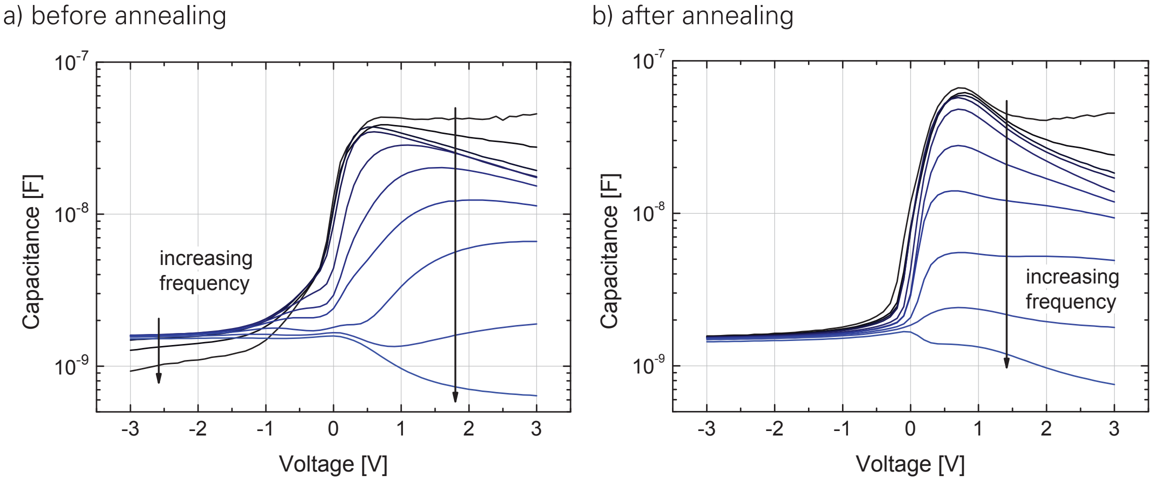

Figure 6.14: Capacitance-voltage measurements of Al / AlO_x / 100 nm C_{60} / 20 nm n-C_{60} / Au / Al at frequencies of 1 kHz, 2 kHz, 5 kHz, 10 kHz, 20 kHz, 50 kHz, 100 kHz, 200 kHz, 500 kHz, 1 MHz. a) before annealing b) after annealing. Capacitance values in backward direction (negative voltages), corresponding to the depletion of the device, do not increase upon annealing as it would be expected by dopant diffusion into the intrinsic region. Furthermore, high capacitances in forward direction reveal the accumulation of electrons in front of the aluminum oxide covering the base electrode with little change after the annealing.

negative voltage leads to a full depletion of the i-C_{60} layer and the capacitance of the diode mainly corresponds to the geometric capacitance of the i-C_{60} layer. This can be seen best for high frequencies since the leakage current from base electrode to the top electrode has a minor influence. In forward direction, positive voltages charge up the i-C_{60} layer, and electrons accumulate in front of the aluminum oxide of the base electrode. The measured capacitance strongly increases to a value given by the geometric capacitance of the AlO_x layer, which can be studied best for low frequencies because residual series resistances limit the time needed to charge the capacitances.

Both features, depletion and accumulation, are found independently whether the device is annealed or not. From this result, two conclusions can be drawn. First, if there would be a significant dopant diffusion into the intrinsic C_{60} region, the depletion of the device towards negative voltages should be delayed. Further, the capacitance at most negative voltages should increase as expected for a decrease in width of the depleted region. The CV characteristic after annealing demonstrates that this is not the case. Between -3 V and -1 V, similar values are reached as before the heat treatment, and the decay of the capacitance towards negative voltages is even more pronounced. Especially in the range between -1 V to 0 V, the capacitance decreases which might be caused by the removal of traps in the C_{60} layer or of interface states at the AlO_x layer. Thus, a dopant diffusion can be excluded, or at least it has a small effect on to the electrical performance of the VOT. Second, the charge accumulation in the device points to the presence of electrons in front of the base electrode, independent of the annealing. As a consequence, at positive bias, charges are present in the emitter layer, ready to be transmitted. If there would be openings in the base electrode before annealing, there should be a transmission of charges from the emitter layer to the collector layer. This means that before annealing the charge carrier transmission is low because the transmission process itself is disturbed, but not due to the absence of charge carriers.

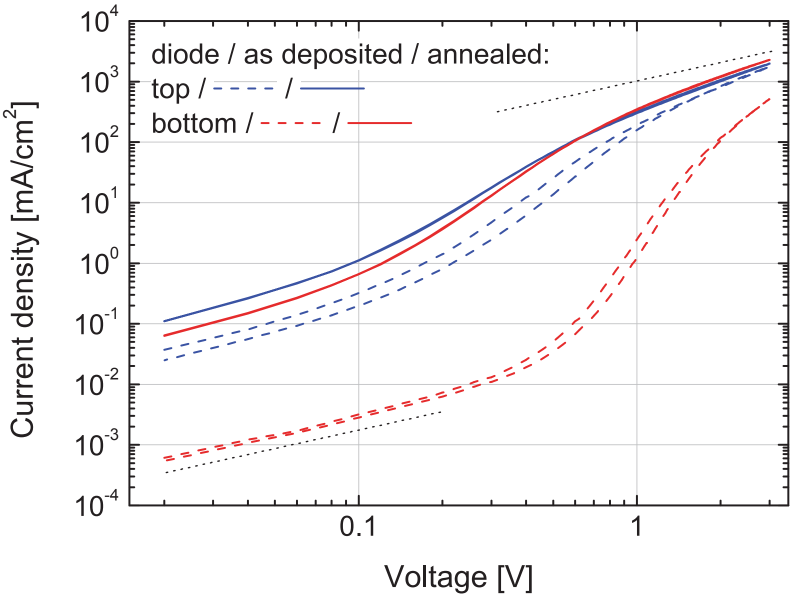

Figure 6.15: Current-voltage characteristics of the top and the bottom diode before and after annealing (2 h at 150 °C). In forward direction, current is injected at the outer electrode and thus represents a leakage current, flowing through the aluminum oxide into the base electrode. The forward and backward sweep of the IV curves reveal a hysteresis for unannealed samples. Dotted lines represent a linear law.

IV characteristics Section 6.2 reveals that the thickness of the oxide, natively built around the Al base electrode, does not grow during annealing. However, it might be that the leakage current, flowing through oxide layer into the base electrode, changes by the heat treatment. For example, a reduction of trap states in the oxide layer might reduce the current flow [450, 529], and in turn the transmission process is influenced by an improved passivation of the base electrode. In order to demonstrate that this is not the reason for the increased charge carrier transmission after annealing, the current flow through the top diode and through the bottom diode is analyzed. The measurement is done in forward direction when charge carriers are injected at the outer contacts and flow through the AlO_x layer into the base electrode, representing an emitter-to-base leakage. The oppositely lying outer electrode is disconnected, so that the respective diode cannot contribute. Figure 6.15 presents the IV characteristic of the top and the bottom diode of a VOT with 100 nm intrinsic layer thickness and a 20 nm doped layer adjacent to each outer electrode. All other fabrication steps are similar to section 5.

As discussed in more detail in Sec. 7.2, the charge accumulation in front of the base electrode leads to a voltage drop mainly across the thin oxide layer. Then, the IV characteristic is mostly influenced by the charge transition from C_{60} through the oxide layer into the base electrode, and measured currents will react most sensitively to changes in the resistance of the aluminum oxide, only limited at the highest currents by the series resistances of the electrodes when the voltages exceeds 1 V. The annealing results in different changes for the top and the bottom diode. For the top diode, currents increase by a factor of 5, and it can be assumed that the leakage current into the base electrode rather increases due to the heating. As a consequence, a change in the resistivity of the oxide layer cannot cause the enhanced charge carrier transmission after annealing. For the bottom diode, the current density increases by two to three orders of magnitude and becomes similar to the top diode after annealing. The main difference to the top diode is that the layers of the bottom diode have been exposed to air. It must be assumed that the air exposure leads to an increased resistivity of the C_{60} layer by incorporating oxygen traps, further supported by the hysteresis of the IV curves before annealing. Similar to the conductivity test shown in Fig. 6.12, the conductivity is restored by annealing. One might argue that the higher resistance of the C_{60} layer used in the bottom collector layer causes the poor charge carrier transmission before annealing. However, an argument against this assumption is the fact that the bottom diode reaches a current density above 100 mA/cm^2 at a voltage of 3 V before annealing. At the same time, common-base measurements with a collector-base voltage of 3 V are not sufficient to realize a high charge carrier transmission even for lower current densities injected at the emitter.

6.7 INTERMEDIATE SUMMARY

This chapter demonstrates that annealing (2 h, 150 °C) is an essential step for the fabrication of working C_{60} triodes. It enables a high charge carrier transmission through the base electrode. At the same time, the native oxide layer, built on the surface of the base electrode upon air exposure, does not show any significant changes, although the leakage current flowing through it slightly increases. Upon applying a base-emitter voltage, it is found that even before annealing, charge carriers are still present in the emitter layer in front of the base electrode, principally capable to be transmitted, but with a low transmission hampered by a lack of pinholes. TEM measurements reveal a lateral increase of the Al crystallites. Smaller crystallites are joined while annealing, implying that the number of crystallites is reduced. As a consequence, small openings form at the grain boundaries with a diameter of only a few nanometers. Therefore, the main reason for the increased charge carrier transmission is the formation of openings within the base electrode, allowing for the direct contact of the upper and lower C_{60} layers. Besides that, the morphology of the bulk C_{60} is stable upon annealing. Neither a reorientation of C_{60} in the bulk layer nor a significant dopant diffusion is observed. However, since trap states can be removed by annealing, an increase of mobility as well as the reactivation of the dopants are further positive features which are improved by the heat treatment. Thus, the annealing has various functions:

1. Pinhole formation due to morphological changes in the base electrode
2. Restoration of the functionality of the dopants for improved charge injection
3. Reduction of hysteresis by removal of oxygen induced traps
4. Increase of charge carrier mobility of C_{60} by removal of oxygen induced traps

As a last point, the idea should be mentioned here that a rearrangement of C_{60} molecules in the pinholes possibly occurs, which supports the direct contact of the upper and lower C_{60} layer.

7 WORKING MECHANISM

The first chapter has revealed how to fabricate a VOT using C_{60} as the semiconducting material. Furthermore, the second chapter demonstrated that annealing is an essential step for device function since it changes the morphology of the base electrode. As a result, openings form which connect the upper to the lower C_{60} layer. Nevertheless, the density of openings within the base electrode seems to be relatively low and their size is likely to remain in the nanometer scale so that the effective area of the openings does not fill more than 1% of the total area. Therefore, it remains unclear, how a transmission in excess of 99% can be explained. For example, the current density of around 1 A/cm^2 injected at the emitter has to pass through the openings. As a consequence, the charges must be transported efficiently to the openings of the base electrode and thus the current density is strongly enhanced in the openings. One reason is that the native oxide surrounding the base electrode acts as a passivation for charge carriers due to its electrically insulating properties. However, this base insulation could also favor the transport of charges to the openings.

In this section, the influence of the native oxide surrounding the base electrode is investigated in more detail. It will be shown that to understand the operation of the whole transistor, it becomes mandatory to study the individual diodes of the device. IV and CV measurements allow to examine the influence of the thin natively built aluminum oxide layer. Different approaches are used to model the diode characteristic. An equivalent circuit is presented to fit the frequency-dependent impedance over the entire voltage and frequency regime and a SPICE (Simulation Program with Integrated Circuit Emphasis) model is used to study the influence of the series as well as the sheet resistance of the base electrode. Drift-diffusion calculations are performed to generate the charge carrier profiles at relevant voltages. Based on these studies, a concise explanation of the operation mechanism can be developed.

7.1 EXPERIMENTAL

Figure 7.1 shows the layer sequence of the VOT. The sample setup is similar to that shown in Sec. 5 with the difference that doped layers are used next to the top and the bottom electrode. As dopant, the highly efficient molecular n-dopant $W_2(hpp)_4$ is used with a doping concentration of 0.5 wt% embedded into the matrix material C_{60}. The device is processed in all combinations of intrinsic layer thicknesses with values of 50 nm, 100 nm, 200 nm, and 400 nm used either in the top diode or in the bottom diode within one single fabrication procedure (c. Sec. 4). Thus, except for the variation of the intrinsic layers, all doped layers and contacts are identical in the devices.

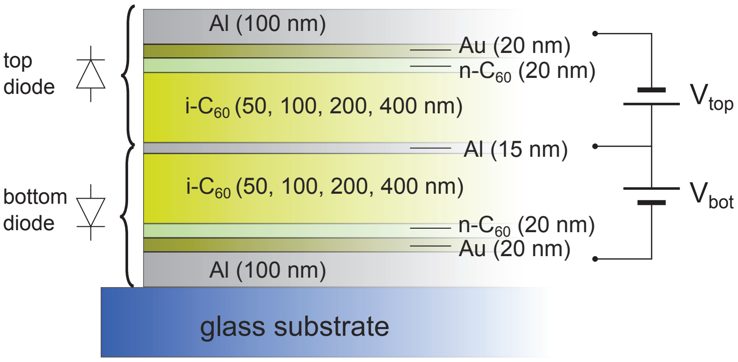

Figure 7.1: Structure of the C_{60} VOT. The device is symmetric with respect to the middle base electrode. The thickness of the intrinsic layers is varied (50 nm, 100 nm, 200 nm, 400 nm) with all possible combinations used in top and bottom diode. For simplicity, the sketch does not show openings in the base electrode which connect upper and lower C_{60} layer.

All samples are produced under high vacuum conditions by thermal vapor deposition. Shadow masks are used to structure the electrodes, while the organic semiconducting layers cover all areas where at least two of the electrodes overlap. The resulting active area defined by the overlap of all three electrodes is approx. 4 mm^2. As specified in Sec. 5 and 6, it is essential to expose the device to air after depositing the base contact, mainly responsible for the formation of a thin native oxide layer on the surface of the base electrode. The completed samples are encapsulated and annealed for 2 h at 170 °C [181]. All CV measurements are done at 1 kHz with a small excitation signal amplitude of 20 mV (rms).

7.2 DIODE CHARACTERISTICS

The key in understanding the operation of the triode is to understand the behavior of the single diodes (c. Fig. 7.1). Therefore, IV as well as CV are measured between one outer electrode and the base contact. The voltage is always applied to the base electrode with reference to the outer electrode, i.e. at positive voltages, electrons are injected from the outer electrode into the adjacent doped layer. The second outer electrode is disconnected, resulting in a potential that suppresses any current flow (e.g. transmission currents) at this contact.

Top diode First, the top diode of the device is discussed. Here, all organic semiconductor layers are processed in vacuum after the air exposure of the base contact. Thus, a minor influence of water and oxygen on these films is expected. Figure 7.2a) presents the IV characteristic. At a forward voltage below 0.5 V, the current grows exponentially. Above this voltage, currents are mainly limited by the influence of the series resistance and by the sheet resistance of the base electrode. In the range of 3 V, current densities larger than 1000 mA/cm^2 are observed. This leakage current represents a direct flow of electrons from the emitter into the base electrode, if measured in the transistor configuration since every increase of base current will diminish the current gain of the triode.

In backward direction, the diode behaves differently. At small negative voltages > -0.5 V, the current starts to rise nearly as strong as for the forward direction, but reaching -0.5 V the current saturates and a clear kink in the curve is visible. The currents in backward direction are due to injection of electrons at the base electrode which will be discussed in Section 7.3 in more detail. At voltages of approx. -3 V, current densities between 1 and 10 mA/cm^2 are reached, leading to a rectification between 100 to 1000.

Most interestingly, the IV characteristics are nearly independent of the thickness of the intrinsic layer, although this thickness is varied by a factor of 8. This can be seen in Fig. 7.2a), showing four curves per device where only the intrinsic layer thickness of the diode is varied. The deviations between different IV measurements are rather related to small but undefined variations in the preparation process than to the systematic variations of intrinsic layer thicknesses.

In principle, two mechanisms determine the current flow: the injection of charge carriers from the metal contact into the device and the transport of charge carriers. Previous investigations on devices with a layer sequence n-doped / intrinsic / n-doped have revealed that i) current densities are much higher in devices without a metallic base electrode, easily reaching values above 10 kA/cm^2 and ii) currents vary by two orders of magnitude with the intrinsic layer thickness even if the thickness of this layer is only changed by a factor of four [318]. Hence, additional factors have to determine the current flow in the diode and injection as well as transport of charges in C_{60} cannot be the main reason for limiting the current.

In order to explain this behavior, Fig. 7.2b) shows the related CV characteristics. In backward direction, a low capacitance arises from the expected geometric capacitance of the intrinsic layer. This is supported by the fact that the capacitance in backward direction scales with the inverse of the intrinsic layer thickness. The formula

$$\frac{C}{A} = \epsilon_r \epsilon_0 \frac{1}{d} \tag{7.1}$$

describes the capacitance C per area A for a parallel plate capacitor with the electrode distance d, the vacuum permittivity ϵ_0 and the relative permittivity ϵ_r. Figure 7.3 shows the capacitance per area over the inverse thickness for the top diode and the bottom diode at a voltage of -3 V where the strongest depletion of the intrinsic layer is reached. The data obeys a linear law corresponding to relative permittivities of C_{60} are 4.0 and 3.3 for the top and the bottom diode, respectively. Differences between both diodes could result from the air exposure changing the density of free electrons in the bottom diode whereas the top diode is assumed to be unaffected [52]. A constant

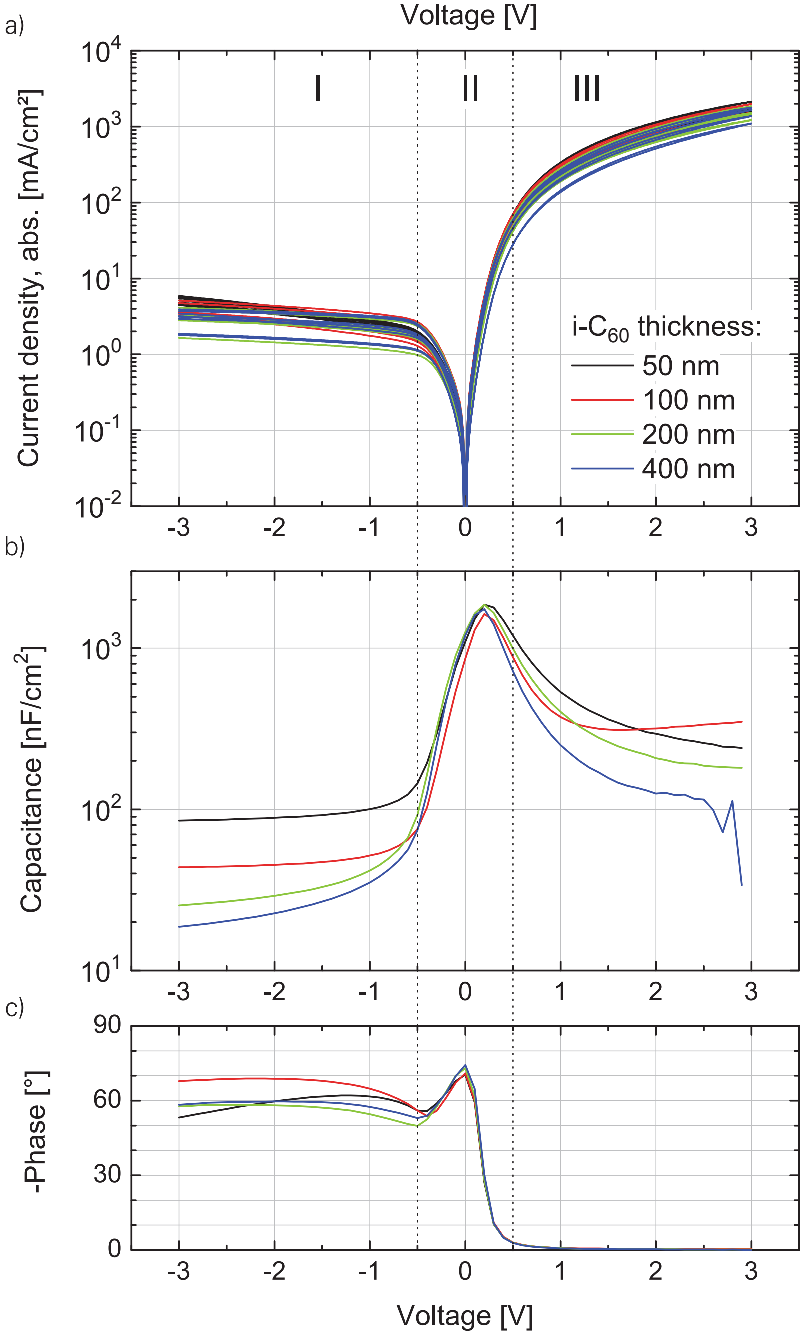

Figure 7.2: Measurement of the top diode. a) IV characteristic with voltage applied to the base contact. Currents are independent of the intrinsic layer thickness. To show variations between samples, four curves measured with forward and backward sweep are plotted with the same intrinsic layer thickness taken from samples which differ by the intrinsic layer thickness of the opposite diode. Differences between samples lie in the range of the variation of intrinsic layer thickness itself. b) CV characteristic ($f = 1$ kHz, $V_{\mathrm{rms}} = 20$ mV), showing a depletion of the intrinsic layer at negative voltages. Around 0 V, charges accumulate at the thin aluminum oxide of the base contact and no intrinsic layer thickness dependency can be obtained. c) Phase-voltage plot. At higher positive voltages, the phase converges to 0°, inhibiting a further evaluation of the capacitance.

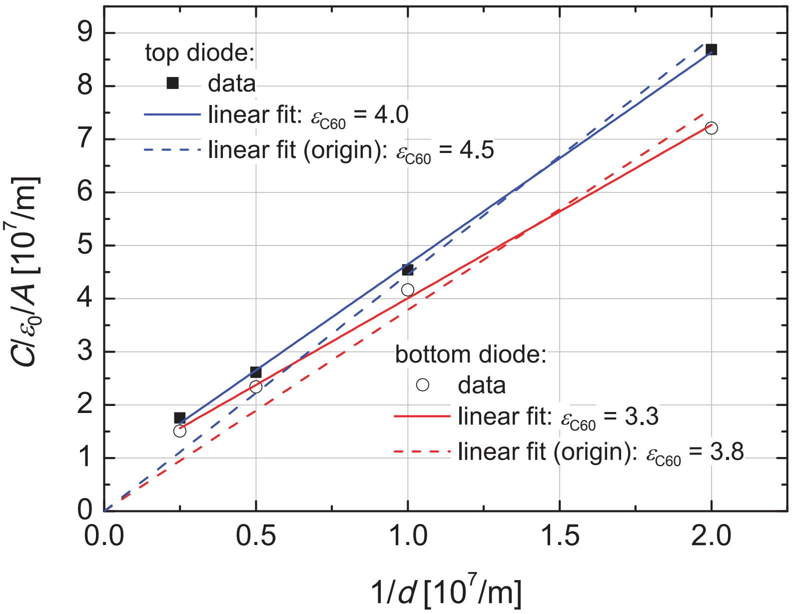

Figure 7.3: Fit of the capacitance at -3 V over inverse intrinsic layer thickness. Depending on a constant capacitance offset, fitted values are in the range between 4.0 and 4.5 for the top diode. Equivalent measurements for the bottom diode lead to values between 3.3 and 3.8 which differ from the top diode. This might be caused by the different quality of the doped layer in the bottom diode (exposed to air) and the top diode (not exposed to air). As a consequence, the profiles of free electrons extending into the intrinsic layer could be influenced.

capacitance offset is added to the fitting procedure, pointing to a residual influence of the oxide capacitance or interface capacitances on the overall capacitance which are independent of the thickness of the organic layer. A fit aligning through the origin deviates from the measurement points and leads to slightly overestimated dielectric constants. For comparison, values obtained in literature are in the range between 4.4 and 5.0 at frequencies between 20 Hz to 1 MHz [323, 411, 432].

In the range between -0.5 V and 0.5 V, the capacitance strongly rises by almost two orders of magnitude. Using Eq. 7.1, this capacitance per area of around 2 µF/cm^{-2} corresponds to the geometric capacitance of a thin native aluminum oxide layer at the base contact with a thickness of 2-3 nm and a relative permittivity of around 8 [479]. This hypothesis is further supported by the finding that around zero voltage, the capacitance does not depend on the intrinsic layer thickness, in contrast to the behavior at voltages below -0.5 V.

Above 0.5 V, the phase ϕ (s. Fig. 7.2c)) drops to values close to 0°. Furthermore, the capacitances seem to drop already before reaching 0.5 V. As will be shown later by simulations, this drop cannot be solely assigned to the influence of the series resistance, but it can be explained if one considers increasing leakage currents flowing through the aluminum oxide layer of the base contact.

Bottom diode Measurements performed for the top diode are now repeated for the bottom diode. In contrast to the top diode, it consists of organic semiconducting layers that are exposed

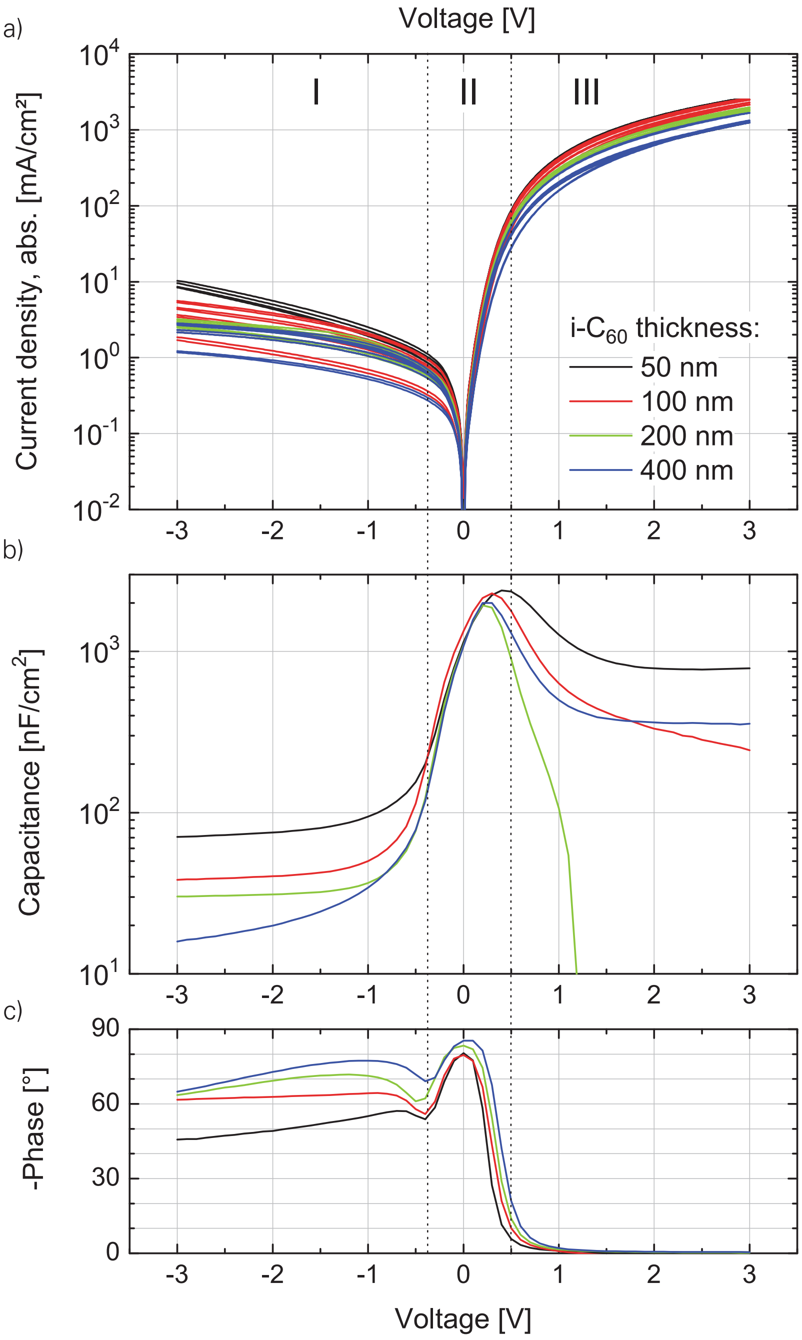

Figure 7.4: Measurement of the bottom diode: a) IV characteristic, showing four curves measured with forward and backward sweep from four different samples for each intrinsic layer thickness similar to Fig. 7.2. b) CV characteristic ($f = 1\,\text{kHz}$, $V_{\text{rms}} = 20\,\text{mV}$). c) Phase-voltage plot.

to air when the vacuum is broken after processing of the base contact. It has to be noted that the dopant $W_2(hpp)_4$ is not stable in air due to its low ionization potential [380, 435]. However, $W_2(hpp)_4$ doping in C_{60} can be regenerated by a subsequent annealing step after air exposure, as shown in Sec. 6 and in Ref. [52].

Figure 7.4 shows the IV characteristics of the bottom diode, the CV characteristics and the corresponding phase. The bottom diode qualitatively exhibits all features discussed for the top diode, although the thickness dependence of the IV curves is slightly more pronounced. The behavior of the diode can be described by three regions with differing voltage ranges. Between -3 V and -0.4 V (region I), the i-C_{60} layer is depleted and therefore the capacitance equals the geometric capacitance of this layer. The electric field will consequently drop across the aluminum oxide layer and the depleted region of the i-C_{60}. In region II defined by voltages between -0.4 V and 0.5 V, the charge carriers accumulate at the interface between i-C_{60} and the aluminum oxide layer of the base contact, leading to very high capacitances similar to the top diode. Therefore, the voltage mainly drops across the aluminum oxide. The CV data implies that this kind of device can be understood as a metal-oxide-semiconductor (MOS) capacitor (cf. Ref. [530]). The aluminum oxide, natively built around the base contact, indeed represents a high capacitance, but exhibits substantial leakage currents. Therefore, in the third region at voltages above 0.5 V, the absolute value of the phase drops to below 10°, and an evaluation of the capacitance is not possible.

Comparing the characteristics of the top and bottom diode, both diodes behave qualitatively similar in all aspects. More specifically, both diodes show current densities exceeding 1000 mA/cm^2 and capacitances remaining independent of the intrinsic layer thicknesses when charge carriers accumulate at the interface between i-C_{60} and the aluminum oxide of the base contact. Most probably, the base contact is oxidized from both sides during air exposure, i.e. the side facing the bottom electrode and the side facing the top electrode as discussed in Sec. 6.4.

7.3 SIMULATION AND MODELING OF THE DIODE CHARACTERISTICS

Three different models are used to understand the behavior of the diode in more detail. The full frequency response of the impedance is measured and discussed in terms of an equivalent circuit model which further proves that measured CV characteristics (cf. Fig.7.2 and 7.4) are valid and that a variation of the depleted region with applied voltage takes place. Further, a SPICE model is applied to evaluate the influence of the series resistance and the sheet resistance. As a last step, drift-diffusion calculations reproduce the experimental results and generate charge carrier and potential profiles present in the diode.

Fit of the impedance spectra In Fig. 7.5a) the Bode plot of the modulus function $|Z|$ is shown for the bottom diode with an intrinsic layer thickness of 100 nm. In a large frequency range, the experimental data follows a 1/f-relation, indicative of the mainly capacitive character of the device. A phase close to -90° is found. In regions with such a high phase, the device capacitance can be

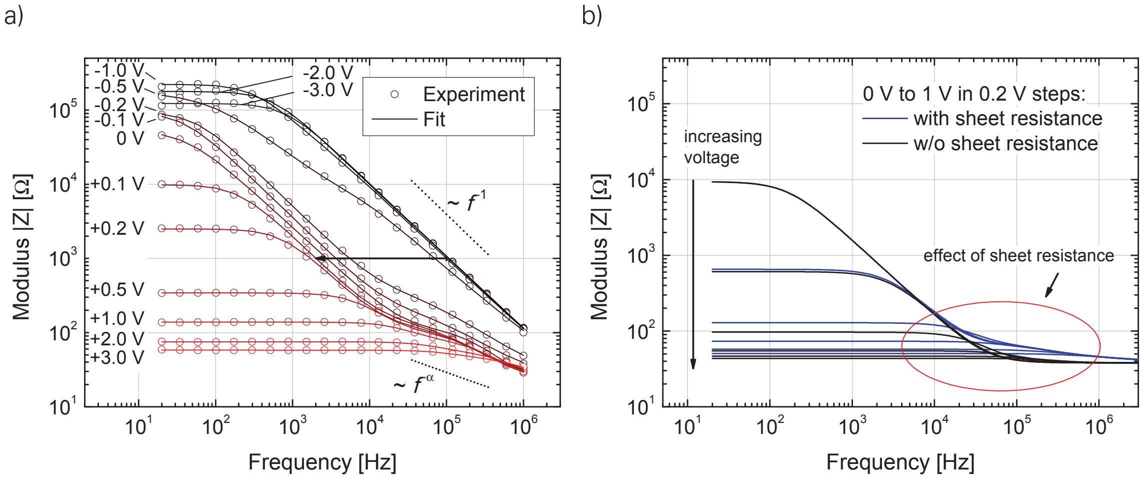

Figure 7.5: a) Impedance-frequency plot for different applied voltages, ranging from -3 V to 3 V. The sample has an intrinsic layer thickness of 100 nm. While switching from negative to positive voltages, the $1/f$ regime shifts about a factor of 50 to the left, indicating a huge increase of capacitance. b) Simulation of the impedance-frequency plot with the SPICE model (cf. Fig. 7.6) for voltages in forward direction, assuming a total oxide capacitance of 100 nF. By changing the sheet resistance value from zero to 75 Ω/sq., a shoulder at frequencies around 100 kHz appears in accordance to the experimental observations.

approximated by $C = (\omega\,|Z|)^{-1}$. For example, the frequency to reach a modulus of 1 kΩ shifts by a factor of 50 to lower values going from -1 V to 0.2 V indicating an increase of the capacitance by a factor of 50. Thus, the frequency-dependent impedance measurements are in accordance to the findings of the previous section. However, at lower frequencies, the data deviates from the purely capacitive behavior, where the modulus saturates. Furthermore, at high frequencies, the modulus drops with $f^{-\alpha}$ $(0 < \alpha < 1)$. Therefore, to model the full experimental frequency range the equivalent circuit model presented in Fig. 7.6a) is used. The equivalent circuit consists of a standard RC element, an RC element using a constant phase element (CPE), and a resistor connected in series. The specific meaning of the series resistance R_S of the device is discussed in the following, but for now a constant value of 22 Ω is chosen for all fits. The first RC element is mainly attributed to the depleted regions within the device and dominates the overall capacitance from -3 V to 0 V. The second circuit element, which is a parallel connection of a resistor and a CPE, is used to achieve a good fitting accuracy at frequencies above 10^4 Hz and voltages above -0.3 V. In principle, the CPE can be seen as a non-ideal capacitance described by the relation $Z \propto f^{-\alpha}$ $(0 < \alpha < 1)$ [319]. At voltages in forward direction, the Bode plot in Fig. 7.5a) exhibits an additional shoulder at frequencies between 10 kHz and 1 MHz. This shoulder is qualitatively reproduced by the CPE. The subsequent section will show that this feature is caused by the sheet resistance of the base electrode.

SPICE circuit for the diode As shown in the previous section, the series resistance limits high currents in forward direction. This seems to be reasonable, since the resistance of the top diode falls below 50 Ω above 1 V and the Al base contact is presumably oxidized from both sides, leading to a non-negligible resistance of this electrode. In order to investigate the effect of the series resistance R_S and the sheet resistance R_{sh} onto the lateral distribution of current and voltage within the diode, simulations are performed using the program LTspice IV (Linear Technology). A

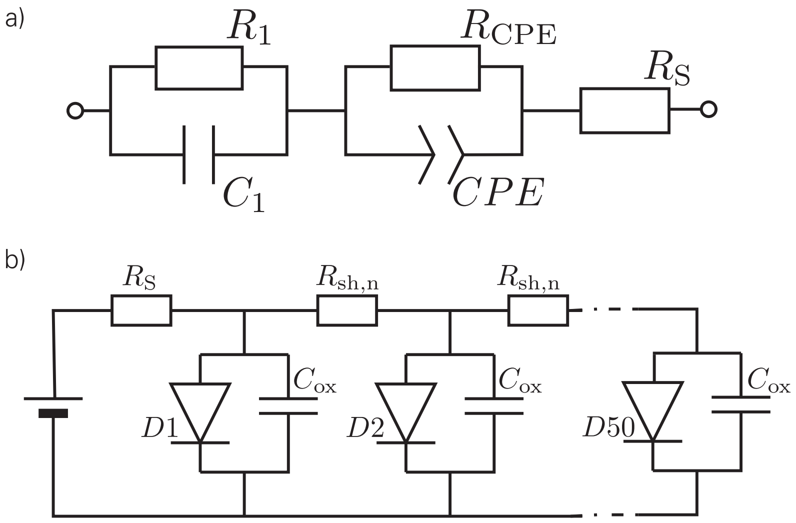

Figure 7.6: (a) Equivalent circuit for the fit of the impedance spectra. (b) SPICE circuit to investigate the influence of the series resistance R_{S} and the sheet resistance R_{sh}.

network is generated to simulate one diode of the VOT as presented in Fig. 7.6b), represented by 50 ideal diodes in parallel (D1, .., D50). Each diode of the SPICE circuit corresponds to a strip-type part of the active area and is described by the following IV characteristic

$$I(U) = I_0(\exp(V/V_0) - 1)/n \tag{7.2}$$

where the current I_0 and the voltage V_0 are fitting parameters and $n = 50$ is the number of diodes. The metallic cathode defines a common reference potential for all diodes, but the oxidized Al anode involves a sheet resistance within the quadratic active area, modeled here with 49 resistors $R_{\mathrm{sh,n}}$, representing the sheet resistance $R_{\mathrm{sh}} = 49 * R_{\mathrm{sh,n}}$. Thus, the voltage drop across the diodes decreases from diode D1 to D50. The voltage is applied to the first diode via a resistor, representing all series resistances given by the setup outside the active area.

The simulation is performed to fit an IV curve of a top diode with an intrinsic layer thickness of 100 nm which is also representative for other samples. Figure 7.7 shows the comparison between experiment and simulation. The parameters of the diodes are adjusted to match the experimental values in the exponential regime in forward direction, where the influence of the series resistance is negligible, using $V_0 = 70\,\mathrm{meV}$ and $I_0 = 7.5\,\mu\mathrm{A}$. In backward direction, these fitting parameters do not lead to a good match to the experimental values, which is not surprising since electron injection from the oxidized aluminum contact into the i-C_{60} layer has to be considered as well. Under the assumption that an exponential relation between current and voltage holds above 0.5 V, an additional series resistance of $R_{\mathrm{S}} = 38\,\Omega$ (black line) can be inserted (cf. Fig 7.6b)) to reduce the calculated current to ca. 40 mA at 3 V (blue line). However, in the range between 0.5 V and 2 V, the current is still slightly overestimated. Introducing a sheet resistance of $R_{\mathrm{sh}} = 75\,\Omega$, the agreement of the calculated current with the observed values is significantly improved in this voltage range. For comparison, measurements of 15 nm Al deposited onto 100 nm C_{60} (oxidized

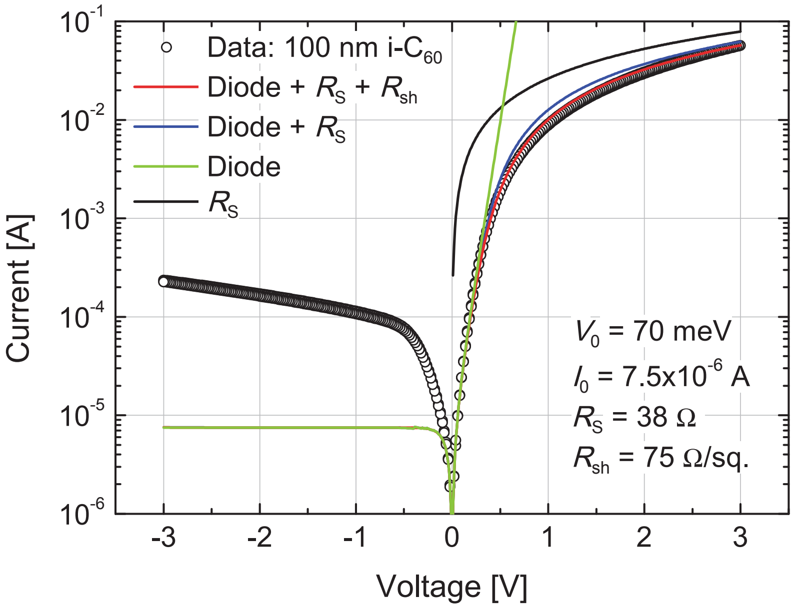

Figure 7.7: SPICE model fitted to measured data. In forward direction, the fit matches the experimental data with the SPICE circuit shown in Fig. 7.6b). At low voltages in forward direction, a diode equation can adequately describe the IV characteristic. Above 0.4 V, a series resistance as well as a sheet resistance are necessary to reach an appropriate description.

and annealed) yielded a sheet resistance of around 30 Ω in the same order of magnitude as the fitted value.

Further, the SPICE circuit can be expanded by additional capacitances in parallel to each of the 50 diodes in order to evaluate the influence of the sheet resistance on the impedance spectra in forward direction (s. Fig. 7.6b)). Since the sheet resistance mainly influences the measurement in forward direction, the capacitance values are chosen equal to the largest capacitance obtained of approx. 100 nF, distributed over the active area in the simulation. Then, the RC time of every capacitance in the SPICE circuit differs due to the sheet resistance. From the simulation, it can be shown that the sheet resistance of $R_{\text{sh}} = 75\,\Omega$ is responsible for an additional shoulder in the modulus-frequency plot at around 100 kHz for voltages between 0 V and 1 V (cf. Fig. 7.5b)), in accordance with the experimental observations (cf. Fig. 7.5a)). A similar system is analyzed by Bisquert to describe the impedance of charge carrier diffusion [531], which leads to $|Z| \propto \omega^{-1/2}$, corresponding to a smaller decay of modulus over frequency with respect to an ideal capacitor. As a consequence, to properly model the interaction between sheet resistances and capacitances, one has to introduce a non-ideal capacitive behavior as well which can be described by a constant phase element, accounting for this distributed property [319]. Thus, the constant phase element used in Fig. 7.6a) correlates with the sheet resistance of the device and it allows to describe the whole frequency dependence of the impedance in Fig. 7.5. Nevertheless, an additional contribution from charge carrier diffusion or trap states on the impedance cannot be fully excluded [531].

Drift-diffusion simulation Next, one-dimensional drift-diffusion simulations are performed with the aim to qualitatively reproduce the experimental results. The simulation model is based on the Scharfetter-Gummel approach [50]. It solves the system of continuity and Poisson equations and describes the current as a superposition of drift and diffusion components. Due to the unipolar character of the diodes in the VOT, only electrons are considered in the calculations. In principle, this approach allows to incorporate modern concepts for charge carrier mobility like the Extended Gaussian Disorder Model whose applicability to organic semiconductors has been demonstrated [106, 532]. However, since a determination of the model parameters is difficult, for simplicity a constant mobility of the individual organic layers is assumed. Similarly, the permittivity of the individual layers is treated as constant, i.e. a possible frequency dependency is ignored. To incorporate energy barriers at the interfaces between adjacent layers in the heterostructure, the tranfer rate expressions for the bulk transport between adjacent sites are altered by exponential factors. That means the rates are multiplied by a term $\exp(-\Delta E/(k_\mathrm{B}T))$ when the barrier ΔE is positive, whereas the bulk rates remain unchanged if the barrier is smaller or equal to zero [106]. Electron injection into n-doped layers is described as ohmic, and the influence of the dopants is represented by a homogeneous and static background charge density. The injection at the base contact of the VOT is described as thermionic, i.e. the applied model [62] accounts for the reduction of the injection barrier by the electric field F and the image charge effect. For a given voltage, independent of the discretization, the simulation model calculates the device current as well as the charge carrier profile n_i.

The capacitance is calculated according to its definition

$$C = \frac{dQ}{dV} \tag{7.3}$$

as the first derivative of the total amount of charges Q with respect to the applied voltage. For this purpose, the charge carrier concentration is integrated in the device volume for a reference voltage and for a voltage lying 10 mV above. The difference of both charges is divided by 10 mV.

To simulate the aluminum oxide layer at the base electrode, an additional intrinsic layer is introduced. It features an energy barrier for electrons to the adjacent semiconducting layer and thus imitates the effective leakage current through the oxide. This is reasonable since the current flowing over an energy barrier can be described by an exponential current-voltage law, as long as the height of the barrier is much greater than $k_\mathrm{B}T$ at room temperature. Such an exponential IV characteristic has also been observed in forward direction of the diode. The effective height of the energy barrier is chosen in a way to realize a similar leakage current flow through the oxide layer as obtained in the experiment. Thus, the detailed transport mechanism through the oxide is not relevant as long as current densities match at similar electric fields.

The device is divided into a sequence of three layers, representing the doped layer, the intrinsic layer, and the oxide layer with layer thicknesses of 20 nm, 100 nm, 3 nm and a relative permittivity of 4.5, 4.5, and 8, respectively[1]. A schematic energy diagram is presented in Fig. 7.8a). The free electron density in the n-doped layer is chosen to be $1 \times 10^{18}\,\mathrm{cm}^{-3}$ while the intrinsic and the oxide layer have no free charge carriers at the beginning. The transport level for electrons

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[1] Sec. 6.4 reveals an oxide thickness of 1.7 nm. However, due to the unknown relative permittivity of the AlOx layer, the thickness in the simulation is set to 3 nm and the relative permittivity to 8 in order to match the capacitance achieved in the experiment.

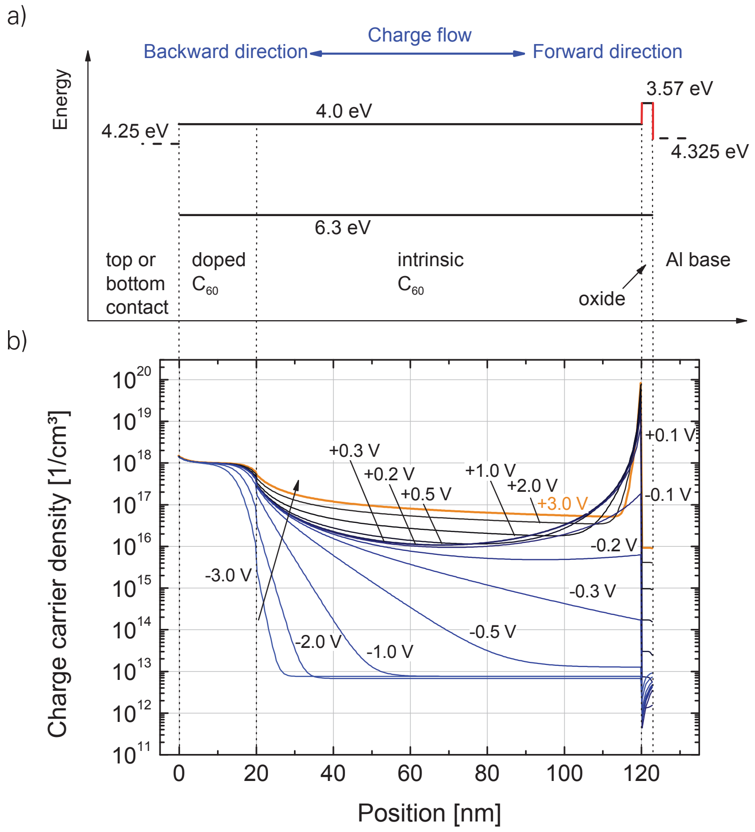

Figure 7.8: a) Schematic energy diagram used in the drift-diffusion simulation. For charge transport in forward direction, the energy barrier between the intrinsic C_{60} layer and the oxide layer is the limiting factor, whereas in backward direction the charge injection barrier between the Al base and the oxide layer plays a dominant role. b) Charge carrier profile for different voltages in a device with 100 nm intrinsic layer thickness. The arrow indicates the increase of applied voltage. The curve for 3.0 V is emphasized in color to show the narrowed accumulation zone.

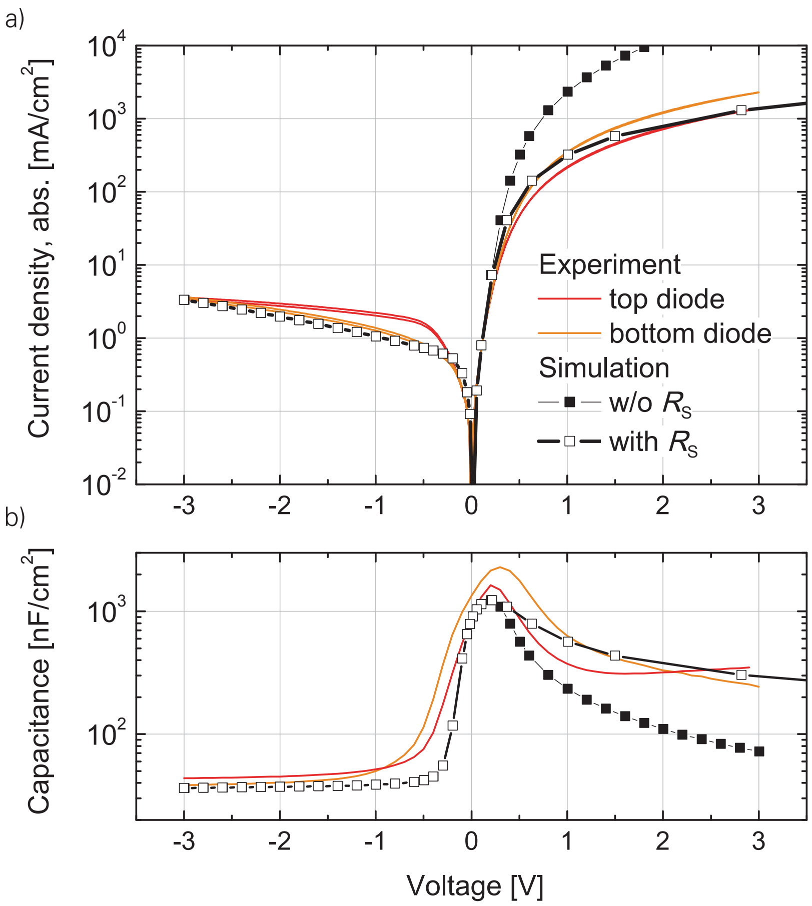

Figure 7.9: Comparison between experiment and simulation for a device with an intrinsic layer thickness of 100 nm. (a) Current-voltage characteristic. (b) Capacitance-voltage characteristic.

in C_{60} is assumed to be at 4.0 eV with respect to the vacuum level [533]. Since hole transport is assumed to be negligible, in all layers the transport level for holes is chosen to be equal to 6.3 eV, introducing a high injection barrier at both contacts and avoiding a significant charge flow of holes. These energy values agree with the LUMO and the HOMO of C_{60} and are used for both the doped and the intrinsic layers. In the oxide layer, electron transport levels are assumed in the simulation at 3.57 eV, introducing an energy barrier for electrons between the intrinsic layer and the oxide layer of 0.43 eV which is significantly larger than $k_B T = 25$ meV. Furthermore, the charge carrier mobility is assumed to be 0.01 cm^2/Vs for all layers [533]. The chosen work function of the Al base contact of 4.325 eV realizes an electron injection barrier to the oxide layer to match the currents of the diode in backward direction. The other electrode has a 0.075 eV lower work function which slightly affects the built-in potential and ensures a better agreement in forward direction. The simulation using this set of parameters, summarized in Fig. 7.8a), matches the measured IV curve in Fig. 7.9 well, i.e. the currents and voltages of the drift-diffusion simulation reproduces the exponential growth at small voltages in forward direction.

Since various configurations of layers and parameters could lead to similar results, the chosen parameters are confirmed further by a comparison of measured and simulated CV characteristics. As shown in Fig. 7.9, the experimental behavior is qualitatively reproduced in all three regions and the basic mechanism can be deduced from the simulated charge carrier profile in Fig. 7.8b).

In backward direction of the diode, the capacitance only depends on the intrinsic layer thickness used in the simulation. For voltages equal to or below -0.5 V, the intrinsic layer is almost completely depleted. The residual plateau of the charge carrier density at $1 \times 10^{13}\,\mathrm{cm^{-3}}$ correlates to the injection of charge carriers from the rectifying contact. For example, calculated current densities in backward direction, given by $j = ne\mu F$, are in accordance with this charge carrier density and the mobility used. Beginning from -0.3 V, the electrons accumulate at the interface between the intrinsic and the oxide layer, accompanied by an increase of the capacitance (cf. Fig. 7.9). Most of the potential drops across the oxide and the charge flow from the C_{60} layer through the oxide into the Al base contact will determine the IV characteristic. Above 0.3 V, the electric field dropping across the oxide layer is sufficiently strong to induce a high leakage current in the range of $\mathrm{A/cm^2}$. In turn, the capacitance decreases since the amount of charges within the device does not rise proportionally with the applied voltage any more. This experimental fact is nicely reproduced by the simulation (cf. Fig. 7.9b)).

However, it is surprising that even for small voltages in backward direction, the charge carrier density already exceeds $1 \times 10^{17}\,\mathrm{cm^{-3}}$ next to the oxide layer. The electric field should deplete the device which however is only seen at larger voltages in backward direction. Also the corresponding capacitance shows an increase already at negative voltages and reaches its maximum at 0.3 V, close to the experimental values. One explanation could be the fact that the intrinsic Fermi level of C_{60} ($\sim 5.15\,\mathrm{eV}$) is far below the work function of the metal used as rectifying contact (4.325 eV). After combining both materials, charges will be transferred from Al to C_{60} to reach a uniform Fermi level, which introduces an electrical field (cf. Fig. 7.10b)) in the thin oxide layer. This layer separates the metal and the organic semiconductor but does not suppress the charge exchange between both. Consequently, these additional charges in front of the oxide are attracted by the Al base contact and thus the simulation shows that slightly higher voltages in opposite direction are necessary to prevent this accumulation of charges in front of the oxide. Investigations by Wilke *et al.* of organic heterojunctions on electrodes with different work functions describe similar observations of charge transfer [534].

The simulation nicely describes the experiment for an applied voltage below 0.5 V (cf. Fig. 7.9), but for voltages above 0.5 V, a series resistance of $30\,\Omega$ is needed to reach a good agreement between simulation and experiment. The series resistance is incorporated by adding the voltage drop over the resistor to the voltage calculated by the simulation for a particular current. In forward direction, corresponding current and capacitance values are shifted to higher voltages. Hence, the simulation does not only match the measured current density above 1 V, but it gives also a realistic capacitance together with their characteristic drop at high voltages. Despite this good accordance, the highest capacitance values measured in the experiment of up to $2\,\mathrm{\mu F cm^{-2}}$ are not reached, since the simulation predicts a decrease of maximum capacitance values by the leakage currents through the oxide layer. However, it should be emphasized that the intention of this simulation is an understanding of the qualitative phenomena taking place in these devices and not an exact reproduction of the measured values. Presumably, the basic assumptions concerning the oxide layer preclude a better quantitative agreement as effects like tunneling or charge transport via defect states are not taken into account.

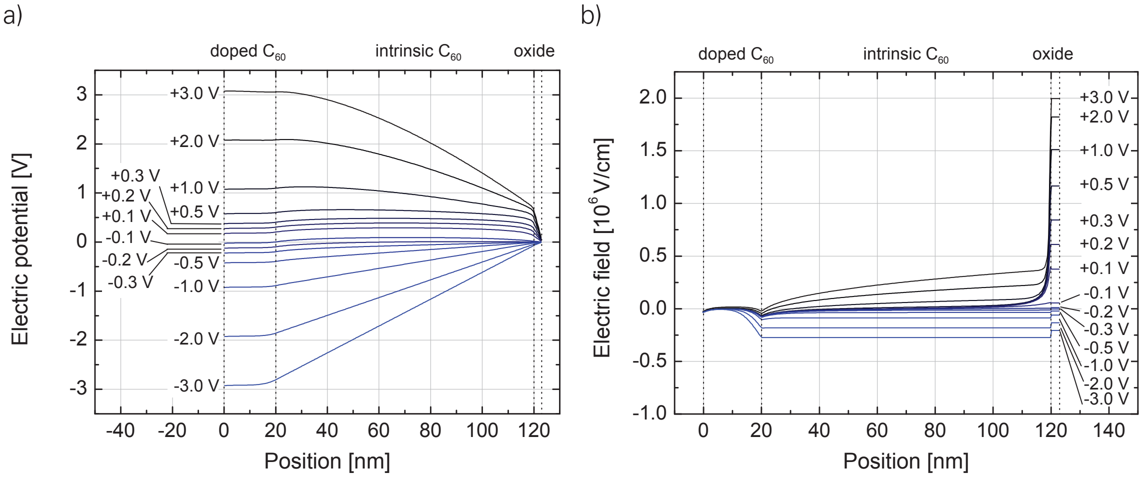

Figure 7.10: Results of the drift-diffusion simulation for a) the potential, and b) the electric field. The applied voltage is varied from backward direction (-3 V) to forward direction (3 V). At low voltages in forward direction (< 0.5 V), most of the voltage drops across the thin oxide, leading to an enhanced electrical field. In contrast to this behavior, the electrical field distributes uniformly over the oxide layer and the depleted intrinsic layer when negative voltages are applied. Only at the interface between both layers an offset due to the discontinuity of the electric field appears.

7.4 INTERPRETATION OF THE OPERATION MECHANISM

The charge accumulation or depletion within the diodes can be used to explain the operation mechanism of the triode, visualized in Fig. 7.11. Normally, the VOT is driven with the emitter diode in forward direction, meaning that a charge accumulation in front of the oxide layer is expected. At the same time, the collector diode is biased in backward direction leading to a depletion on the side of the base electrode facing the collector.

In our present understanding of this device, the base electrode is a continuous, but not fully closed layer with small openings enabling direct contact between the upper and the lower C_{60} layers. If one of these layers exhibits a charge accumulation and the other layer is nearly depleted, a huge gradient in charge carrier concentration develops across the openings of the base electrode. Thus, the overall transmission current should contain a strong contribution of diffusion currents through these pinholes. Furthermore, the simulation reveals that the electric potential is enhanced in front of the oxide layer with respect to the corresponding collector region as shown in Fig. 7.10. Consequently, besides the large diffusion current, a drift current contributes to the total emitter-collector current.

Of course, the transmission of charge carriers reduces the charge concentration in front of an opening of the base contact. Hence, a carrier gradient develops in lateral direction around each pinhole, leading to a diffusion as well as a drift charge transport towards the pinhole (cf. Fig. 7.11). Thus, the accumulation zone can be interpreted as a 2D charge channel which effectively transports charges to the pinholes of the base electrode and enables a high transmission of charge carriers close to 100%. In this sense, the electrical feedback between emitter and collector, as revealed in Sec. 5, has to be understood as a complex interaction between the contacts and the accumulation zone. Presumably, the collector potential will modify the electrical field at the

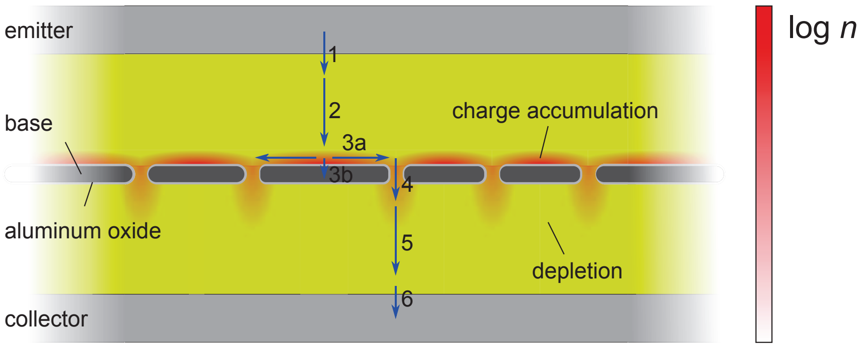

Figure 7.11: Visualization of the operation mechanism. Red color represents schematically a high charge carrier concentration as expected for the accumulation zone under operation. Blue arrows show the motion paths of charge carriers: (1) injection at the emitter, (2) transport through the intrinsic emitter layer, (3a) lateral transport within the accumulation zone, (3b) leakage current into the base electrode, (4) transmission through a pinhole, (5) transport through the intrinsic collector layer, (6) ejection at the collector.

emitter contact by changing the charge carrier distribution within the 2D charge channel. To gain further insight, two-dimensional drift-diffusion simulation would be the tool of choice. Thus, the current flow in front of the base electrode can be visualized, allowing to estimate which pinhole concentration and size is necessary to reproduce the measured current densities in the on-state. Especially, if a similar leakage current density of the native oxide layer is used, it will be of interest whether similar current gains can be reproduced. Such work could be part of further investigations continuing the progress in the field of Vertical Organic Triodes.

7.5 INTERMEDIATE SUMMARY

A vertical organic transistor with a permeable base electrode has been analyzed in terms of capacitance and current-voltage characteristics of the single diodes connected in these devices as well as of the whole transistor structure. In forward direction, one observes a strong charge accumulation in the diodes, while in backward direction, a depletion of the intrinsic layer occurs. The reason for this behavior is a native oxide layer on the surface of the permeable base electrode which is realized by air exposure after processing of this Al contact. Thus, the two diodes of the VOT can be interpreted as MOS diodes back-to-back, connected by small openings in the shared base contact. As a consequence, large diffusion currents contribute to very large transmission current densities of 1000 mA/cm^2 at driving voltages of only 1 V. These results give a microscopic picture of the operation mechanism of the VOT which will help to focus on relevant optimization steps. There is still ample space for improvement in terms of on/off ratio and current gain if the passivation of the base electrode can be significantly improved without hindering the pinhole formation.

8 OPTIMIZATION OF VOTS

This chapter demonstrates the opportunities for further device optimization. It will be discussed which processes limit the performance and which device parameters can be improved. Although C_{60} VOTs have high current densities at low driving voltage, they suffer from a small on/off ratio and a small current gain, indeed comparable to inorganic bipolar transistors, but too low for several applications typical for OFETs. Here, various approaches to optimize triodes are presented which are not solely applicable to C_{60} triodes. Parts of this section are published in Ref. [181].

8.1 MISALIGNMENT OF THE ELECTRODES

Before first optimization steps are presented, the mask alignment and any problem arising from slightly misplaced masks are discussed. It will be shown that the triode is limited by the low alignment accuracy. The setup used in this work has a rather large mask displacement in the range of 200 μm which is around 10% of the edge length of the active area. If all electrodes are designed to exactly align in the active area, even a small misalignment easily leads to parts of the triode where emitter and collector are facing each other, i.e. the base is not able to modulate the current flow there. In this area, the resulting device consists of n-doped / intrinsic / n-doped layers. The current in such nin-devices is typically limited by space charges only and the current density can easily reach 10 to 100 times higher currents than reached in the on-state of the C_{60} triodes [318]. As a consequence, the current in the off-state would strongly rise and lower the on/off ratio. To solve this problem, the base electrode is designed to have a larger width so that even with misalignment, the emitter and collector electrode are always separated by the base electrode. However, this method introduces other kinds of misalignment which can be handled easier or which are negligible.

Figure 8.1 shows a schematic cross-section of a vertical organic triode and the different regions of electrode overlap. First, the active area A is defined by the overlap of all three electrodes (region II). Moreover, there exists an area A_{BC} where base and collector electrode overlap (region I) as well as an area where emitter and base overlap (region III). For both areas, an alignment factor

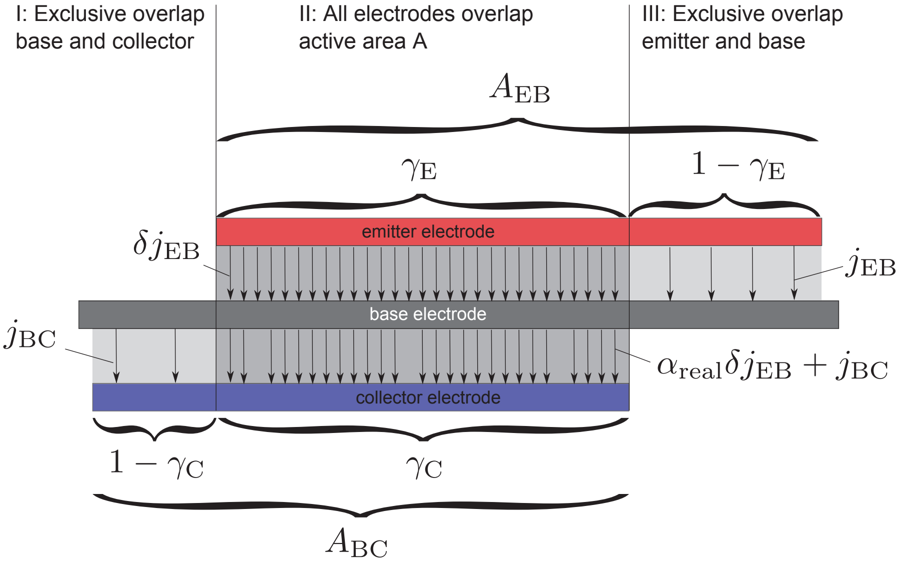

Figure 8.1: The schematic cross-section of the VOT visualizes electrode overlaps and the different current densities which occur in the device.

can be defined as

$$\gamma_{\mathrm{C}}=\frac{A}{A_{\mathrm{BC}}} \quad \text{and} \quad \gamma_{\mathrm{E}}=\frac{A}{A_{\mathrm{EB}}} \tag{8.1}$$

which specifies the amount of base-collector overlap or base-emitter overlap contributing to the active area where a transmission current can flow. For example $\gamma_{\mathrm{E}}=0.9$ means that 90% of the overlap of base and emitter electrode is part of the active area. Measurements of the electrode alignment after fabrication of the samples reveal that the typical alignment is in the range of 85% to 90% for both, the emitter and the collector. These misalignments have a different influence on the performance of the VOT. A misalignment in region I leads to an enhanced area where current of the base-collector diode flows in backward direction and increases the off-state current whereas the on-state current is not affected. In comparison to a perfectly aligned sample, the on/off ratio is consequently decreased by a factor $1/\gamma_{\mathrm{C}}$. Since the on/off ratio should be several orders of magnitude, a slight decrease of the on/off ratio by less than a factor of 2 due to misalignment is acceptable and thus this kind of misalignment is not relevant.

Region III where emitter and base electrode overlap exclusively is more complicated. The problem arises due to the leakage current from the emitter through the native oxide into the base (cf. Sec. 7.2). In the whole misaligned area, injected charge carriers at the emitter which are transmitted cannot be collected because of the absence of the collector electrode and the current in this region

$$I_{\mathrm{III}}=j_{\mathrm{EB}}(1-\gamma_{\mathrm{E}})A_{\mathrm{EB}} \tag{8.2}$$

completely drops into the base electrode where j_{EB} equals the current density in this area. As a result, the measurable transmission factor α_{meas} is reduced since a part of the injected emitter current is contributing to the base current. It is mandatory to keep these losses as small as possible because the current gain quickly drops with a reduced transmission factor. For instance, if there is an alignment of $\gamma_{\mathrm{E}}=0.9$, the maximum measurable transmission cannot be higher than

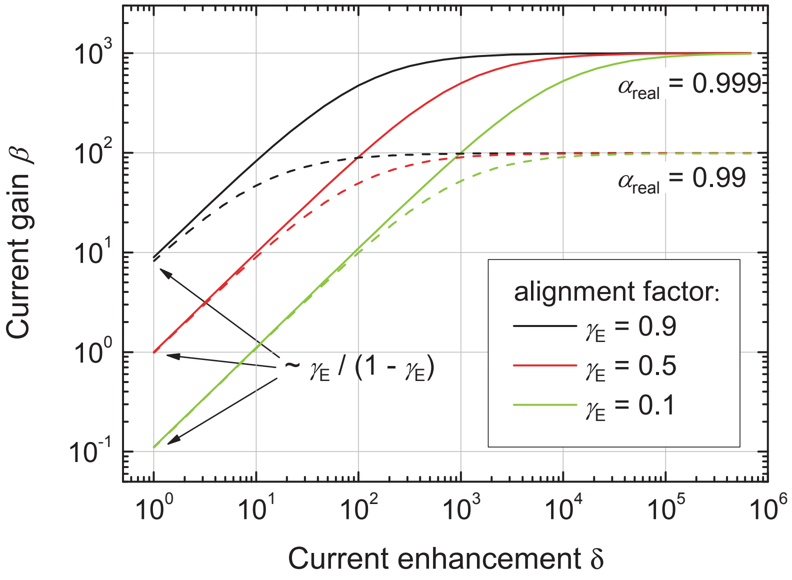

Figure 8.2: Current gain as a function of the current enhancement between aligned and misaligned areas for different alignment factors and real transmission factors α_{real}.

90% and the current gain cannot exceed 9. The given example relies on the assumption that the current density in the emitter-base diode is equal in both regions, in the active area where a majority of the charge carriers is transmitted and in the misaligned area where all charges drop into the base electrode. Hence, it is reasonable to assume that the measured current gain of the VOTs is already limited by the misalignment of the electrodes.

Influence of current enhancement The situation changes if the current density is enhanced in the active areas. In this case, the aligned and misaligned area do not proportionally contribute anymore to the overall emitter current. The reason for a current enhancement is discussed in Sec. 5. An electrical feedback develops between emitter and collector which leads to an enhanced transmission current. The collector potential influences the distribution of the electrical field in the emitter layer via the openings of the base electrode and thus can increase the injected current at the emitter. This mechanism is a unique feature present in the active area and cannot occur in the misaligned areas. Therefore, the current density is higher by a factor $\delta > 1$ in the active area than in all other regions, if a transmission current flows.

The remaining question is: For which current enhancement factors and which alignment factors would it be possible to measure a transmission α_{meas} which is close to the real transmission α_{real} defined as the value which can be actually realized as an intrinsic feature of the permeable base electrode. To calculate the relation between the real and the measurable transmission, the transmitted current has to be compared with the current injected at the emitter. The emitter current

$$I_E = \delta j_{EB} \gamma_E A_{EB} + (1 - \gamma_E) j_{EB} A_{EB} \tag{8.3}$$

consists of a first part injected in the active area and a second part injected in the misaligned area. The transmission current is then

$$I_T = \alpha_{\text{real}} \delta j_{EB} \gamma_E A_{EB} \tag{8.4}$$

reduced by the real transmission value α_{real} with respect to the injected current within the active area. Finally, the measured transmission

$$\alpha_{\text{meas}} = \frac{|I_T + I_{BC|}}{|I_E|} = \frac{1}{1 + \frac{1}{\delta}\left(\frac{1}{\gamma_E} - 1\right)} \alpha_{\text{real}} \tag{8.5}$$

can be expressed as a function of the real transmission. In Fig. 8.2, the corresponding current gain

$$\beta = \frac{\alpha_{\text{meas}}}{1 - \alpha_{\text{meas}}} \tag{8.6}$$

is visualized as a function of the current enhancement for different alignment factors (γ_E = 0.1,0.5, and 0.9) and two different real transmission factors (α_{real} = 0.99 and 0.999). If the current enhancement is not present or very small ($\delta \sim 1$), the current gain is limited by the misalignment. This can be seen by the fact that the current gain is directly related to the current enhancement whereas a change of the real transmission factor does not influence the position of the curve (cf. Fig. 8.2). The situation changes if the current enhancement is between 10^2 and 10^3 and the current gain starts to saturate. The current enhancement is now so high that the contribution of current flow from misaligned areas does not influence the measurable current gain anymore. However, the required current enhancement depends on the misalignment and the current gain which should be reached, i.e. to reach a current gain close to the maximum value for $\alpha_{\text{real}} = 0.99$ and $\gamma_E = 0.5$, a δ of 10^3 is necessary.

In contrast to a limitation of the measurable transmission due to misalignment, currents in backward direction of the base-collector diode lead to the measurement of an increased transmission value. As these leakage currents are, however, typically small and not modified by the current enhancement, the current of the base-collector diode is assumed to be negligible.

8.2 USE OF DOPING

Improvement of injection Previous investigations have been performed with C_{60} triodes involving doped layers. Here, the role of doping will be discussed in more detail. Typically, doped layers are used to ensure an Ohmic injection from an electrode, e.g. a metal to a semiconductor [51]. For a triode, this condition is required for the emitter contact, since the transmitted current cannot be higher than the current injected into the device. In Fig. 8.3, base sweep measurements for a sample with and without a doped layer are compared. The sample configuration is similar to that of Sec. 5. The doped layer is inserted close to the top electrode used as the emitter and the driving voltage is 3 V.

The most essential improvement by using a doped injection layer is the increase of the on-state current density by one order of magnitude to around 1000 mA/cm^2. Although the charge injection

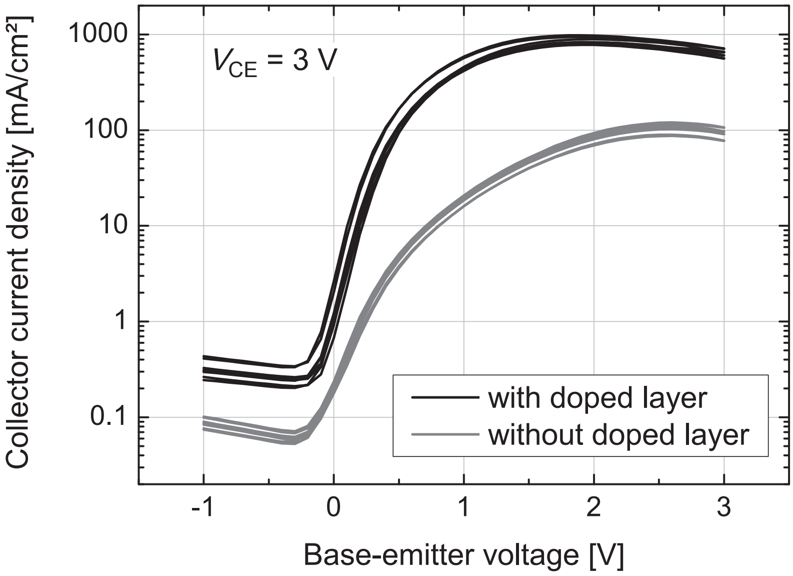

Figure 8.3: Base sweep measurements at a driving voltage of 3 V for a sample with and without a 20 nm thick doped layer close to the emitter layer. The doped layer reduces the injection resistance and enables higher current densities up to 1000 mA/cm^2.

from the Au layer of the top electrode into the intrinsic C_{60} leads to remarkable current density of 100 mA/cm^2, it can be still enhanced by the use of a doped layer. At the same time, this modification will influence the transconductance of the device which increases from 3 mS to around 30 mS. Furthermore, the subthreshold swing is decreased from 280 mV/decade (undoped) to 200 mV/decade (doped). This change can be explained by a faster transition from a depletion to accumulation mode in the base-emitter diode. Although these improvements are significant, the full potential of doping will become apparent if organic semiconductors are used which form Schottky-barriers to the most common metals or suffer from a bad charge injection. Then, doping is essential to realize devices working at low driving voltages similar to OLEDs or OSCs [51]. In contrast to OFETs, doped layers can be easily inserted in VOTs, just by adding a further layer to the stack. Indeed, top contact OFETs can be improved by using the shadow mask of the source/drain contacts to add a structured doped layer but high resolution structuring is impeded. Bottom contact OFETs have the advantage that their source/drain contacts can be made by high resolution photolithography due to the absence of any organic thin film. However, it is difficult to align a further doped organic layer with the source/drain contacts which is why several scientific groups try to functionalize the electrode with self-assembled monolayers [535–537].

Current gain The improvements discussed above are similar to those achieved for inorganic bipolar transistors where the emitter layer is highly doped [3]. However, the C_{60} triodes presented in this work show a considerable enhancement of the current gain by inserting a doped injection layer. Figure 8.4 visualizes the differential current gain over the base-emitter voltage (a) and the collector current density (b). By using a doped injection layer, the highest current gain increases by a factor of ten, and compared to a high collector current density of around 100 mA/cm^2, the performance improves even more. This effect can be explained if one considers the dependency of the misalignment of the electrodes and the current enhancement in the active area due to the feedback between collector and emitter. The electrode alignment has been evaluated by

a) b)

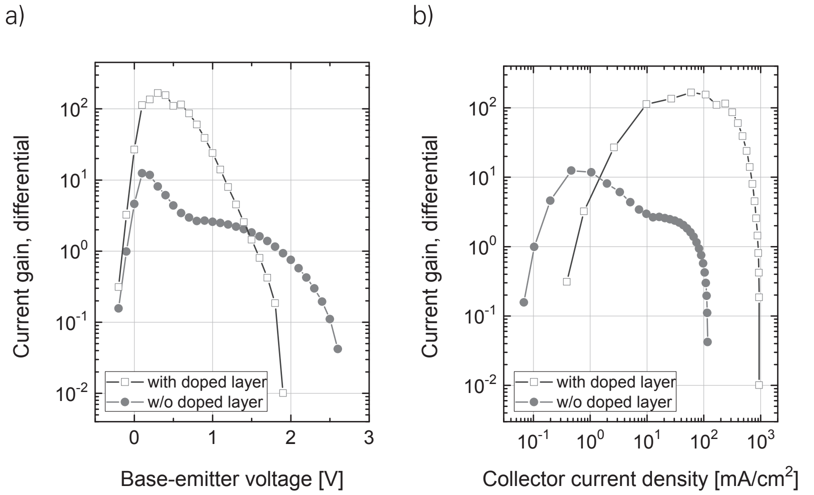

Figure 8.4: a) Differential current gain vs. base-emitter voltage. b) Differential current gain vs. collector current density. A doped layer at the emitter contact realizes an enhanced current injection. As a consequence, higher current gains at higher current densities are reached.

comparing an optical picture with the layout of the electrodes and the analysis shows that the alignment factor of the emitter γ_E is not greater than 85%. If a homogeneous current flow in the emitter layer is assumed, the current gain cannot be higher than 6 according to Eqs. 8.5 and 8.6. Besides that, due to the slightly larger width of the base electrode, the alignment factor is limited to a maximum of 0.95 which equals a current gain of 20. In contrast, the differential current gain clearly exceeds 100 for a sample with a doped injection layer at the emitter. This contradiction implies that there cannot be a homogeneous current flow in the sample. Higher values can only be reached if the current is enhanced in the active area with respect to the misaligned areas of the base and the emitter as explained in Sec. 8.1.

Fortunately, the current enhancement can be experimentally determined by measuring the emitter current of the VOT and the current of the base-emitter diode with disconnected collector for the same base-emitter voltages. While the emitter current can be enhanced due to the transmission of charges through the base electrode, this would not be possible if the collector is disconnected. Corresponding measurements for a sample with and without a doped injection layer at the emitter are shown in Fig. 8.5a). It becomes obvious that the current injected at the emitter of the undoped VOT is less influenced by additional transmission currents whereas a doped VOT gains additional emitter current due to the transmission process. The current enhancement in the active area of the emitter region is calculated by

$$\delta = \frac{I_E - I_{BE}(1-\gamma_E)}{\gamma_E I_{BE}}, \tag{8.7}$$

taking into account that a part of the measured emitter current is still flowing in the misaligned region. Figure 8.5b) compares calculated values for both samples. The doped sample has always a current enhancement above 2, in contrast to an undoped sample where it quickly drops to 1. It can be assumed that both samples have a similar permeable base electrode since the doped layer is processed after the second intrinsic C_{60} layer, so that an influence on the morphology of the base electrode is excluded. In a sample with low contact resistance (doped), the native oxide of the base electrode limits the current flow of the base-emitter diode. Moreover, Fig. 8.5a)

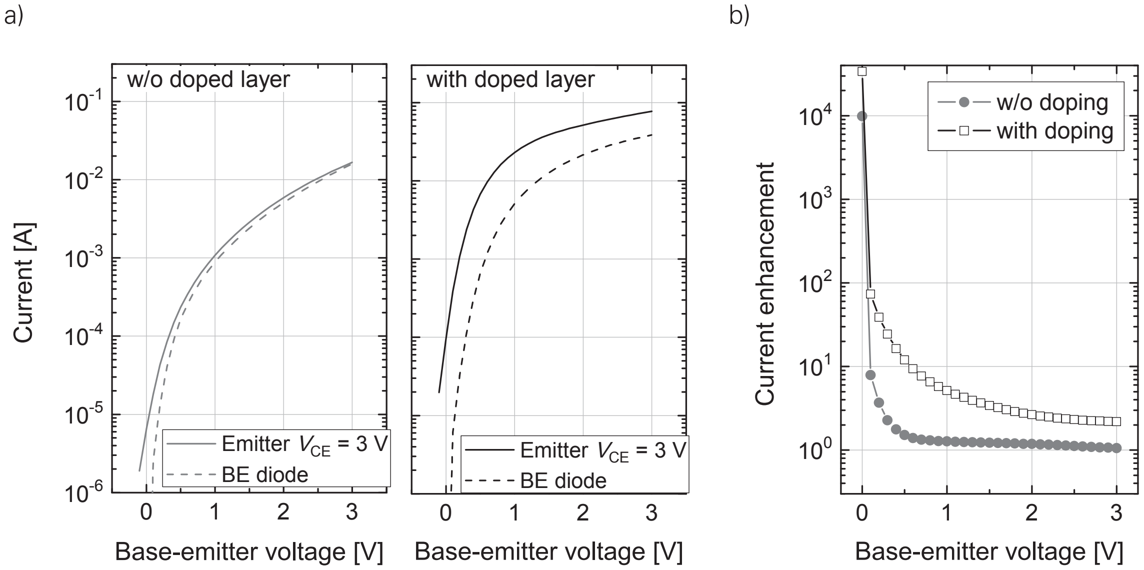

Figure 8.5: Comparison of the current enhancement of a triode with an active area of ca. 4 mm^2. a) Emitter current at a driving voltage of 3 V compared with the current flowing in the base-emitter diode with disconnected collector for a sample with and without doped layer at the emitter. b) In case of transmission, the current in the active region is enhanced. The effect is stronger for a sample with a doped layer where, due to the lowered contact resistance at the emitter electrode, the feedback between collector and emitter has a stronger impact.

reveals that the current of the base-emitter diode is lower if no doped injection layer is present. Then, an additional contact resistance limits the current flow. If a feedback between collector and emitter exists, it leads to an increased electric field in the emitter layer. Depending on the contact resistance, the emitter current increases and results in an enhanced current of the active area.

An interesting feature is that for both samples, the current enhancement rises to infinity at base-emitter voltages close to 0 V, with and without doped layer. If no voltage between the emitter and the base is applied, no current can flow in misaligned areas. In the active area, however, a transmission current flows due to the feedback between collector and emitter. As a consequence, this potential configuration allows to measure the transmission without a disturbing influence of the misalignment. Nevertheless, the highest current gain is measured at base-emitter voltages slightly above 0 V, since current in backward direction of the base-collector diode prevents a correct determination of the current gain. With that knowledge, the peak in Fig. 8.4a) of the current gain at around 0.1 V in the undoped triode can be interpreted. The higher current gain of the peak is a result of the higher current enhancement in this voltage range, but it quickly vanishes with the drop of the current enhancement. For the doped sample, the higher current enhancement enables to measure higher current gains of up to 160 at $V_{\mathrm{BE}} = 0.5\,\mathrm{V}$, much larger than the value predicted by the alignment factor for a homogeneous current flow. As a result, it is shown that the current gain is a parameter highly depending on the mask alignment and thus a comparison of published current gains has to be treated with caution whenever this alignment problem is not addressed.

8.3 VARIATION OF THE INTRINSIC LAYER THICKNESS

Substantial improvements can be achieved by decreasing the intrinsic layer thickness of both, emitter and collector side. In the following, the sample structure of the Sec. 7 is used where doped injection layers are inserted close to the top and the bottom electrode. The intrinsic layer thickness in the top or bottom diode is varied from 50 nm to 400 nm.

Emitter side The influence of the intrinsic emitter layer thickness can be shown best in a base sweep as presented in Fig. 8.6a). The driving voltage is kept constant at $V_{\mathrm{CE}} = 1\,\mathrm{V}$. In the on-state at a base-emitter voltage of 1 V, the current densities are dropping with increasing intrinsic emitter layer thickness by a factor of 2. This indicates that the transmission current in the on-state is not exclusively limited by transmission process through the openings of the base electrode. The on-state resistance also depends on the resistance of the intrinsic emitter layer, introducing a resistance given due to charge transport. However, the variation of the on-state current density is rather low compared with the strong variation of intrinsic layer thickness and thus it can be concluded that either the transmission process or a residual series resistance outside the device mainly limits the current flow. Please note that intrinsic layers indeed have a low intrinsic charge carrier concentration but if the diodes of the VOTs are biased in forward direction, the injected charge carriers as well as the charge accumulation lead to a significant rise of free charge carriers in the intrinsic layer which in turn drastically reduce the resistance of the layer. Furthermore, no shift of the onset of the current rise is visible which is in accordance with the CV measurements of the top diode in Sec. 7.2. The rise of the capacitance with the accumulation of charge carriers at the oxide of the base electrode setting in does as well not depend on the thickness of the intrinsic layer thickness. Nevertheless, VOTs with a higher built-in potential of the base-emitter diode could show a stronger dependence of the intrinsic layer thickness. Here, at an applied voltage lower than the built-in potential, solely diffusion currents can contribute to the overall current flow and thus a relation between diffusion length and intrinsic layer thickness is likely.

Collector side The effect of the intrinsic collector layer thickness is shown in Fig. 8.6b) for a common-base configuration with a constant emitter current of $I_{\mathrm{E}} = -10\,\mathrm{mA}$ and a constant intrinsic emitter layer thickness of 50 nm. Thus, one can expect that the charge accumulation in front of the base electrode is similar for all samples if no transmission current occurs and that the transmission current is mainly influenced by the thickness of the intrinsic collector layer. With increasing thickness of this layer, the voltage necessary for reaching a collector current equal to the injected emitter current increases. The electric field dropping over the intrinsic collector layer also decreases with layer thickness, leading to an insufficient charge transport through and away from the openings of the base electrode. Thus, it is most efficient to keep the intrinsic collector layer thickness as thin as possible but as thick as necessary to prevent short cuts between the base and the collector electrode in the fabrication process. Then, the highest current gains at the lowest driving voltages can be obtained. In some cases, it might be appropriate to use a larger layer thickness, e.g. to apply higher voltages before the dielectric breakdown occurs or to influence the strength of the feedback between collector and emitter. A lower electrical field in the base-collector diode could also positively influence the on/off ratio by reducing the current in

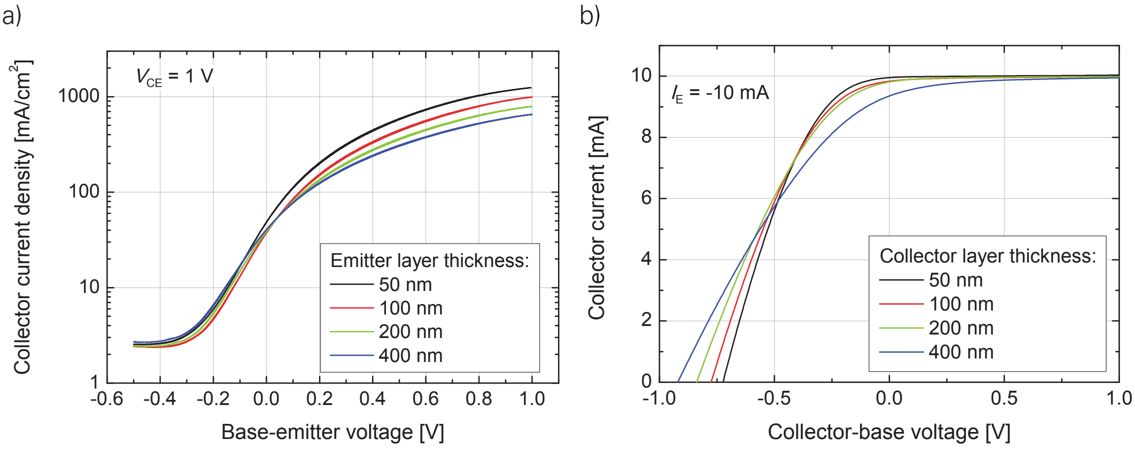

Figure 8.6: Transistor characteristics using the top electrode as the emitter. a) Variation of the intrinsic emitter layer thickness from 50 nm to 400 nm whereas the thickness of the intrinsic collector layer is kept constant at 50 nm. In a base sweep measurement with $V_{CE} = 1$ V, the current in the on-state is increased by a factor of 2 with decreasing layer thickness. b) Variation of the intrinsic collector layer thickness from 50 nm to 400 nm whereas the thickness of the intrinsic emitter layer is kept constant at 50 nm. The current injected at the emitter is kept at I_E = -10 mA (j_E = -250 mA/cm^2).

backward direction of the BC diode. As revealed in Sec. 7.2, the diodes used in the C_{60} triode show a less pronounced thickness dependence so that an increase in intrinsic layer thickness is not convenient.

Bidirectional transistor operation The variation of the intrinsic layer thickness above reveals that the device works most efficiently if this thickness is as small as possible, but large enough to prevent electrical shorts. By choosing the optimized thickness of the emitter and collector layer of 50 nm and using doping on both outer electrodes, C_{60}VOTs are fully symmetric to the base electrode regarding the layer stack. Thus, the performance of both operation directions, emitting charges from the top or the bottom electrode, can be compared in detail. In Fig. 8.7 the voltage applied between base electrode and emitter electrode is swept from -0.5 V to 1 V in a common-emitter configuration (base sweep), using the top electrode (Fig. 8.7a)) or the bottom electrode as the emitter (Fig. 8.7b)). In this measurement, the transistor switches between off-state and on-state at very small base and collector voltages (both 1V only, c. ref. [181, 182]). The off-state is reached at negative voltages between base and emitter for both operation directions, clearly limited by the current flowing from base to collector (BC diode), whereas the on-state is reached at positive base-emitter voltages. These devices are able to reach 1000 mA/cm^2 at a driving voltage of 1 V, irrespective of the operation direction. Considering an active area of 4 mm^2, the total resistance of these transistor structures remains below 25 Ω which is close to the resistance of the electrodes outside the device. Thus, outstanding transconductances for organic transistors are realized, reaching 60 mS with the top electrode as emitter and about 95 mS with the bottom electrode as emitter. In comparison to the ideal transconductance of an inorganic bipolar transistor, 385 mS at 10 mA, the performance of the VOT only differs by less than one order of magnitude [3]. Both transistors can be well compared since they have their highest transconductance at ca. 10 mA. In contrast, OFETs are have much lower currents and the highest transconductance is reached in the µA range. For example, a state-of-the-art device with

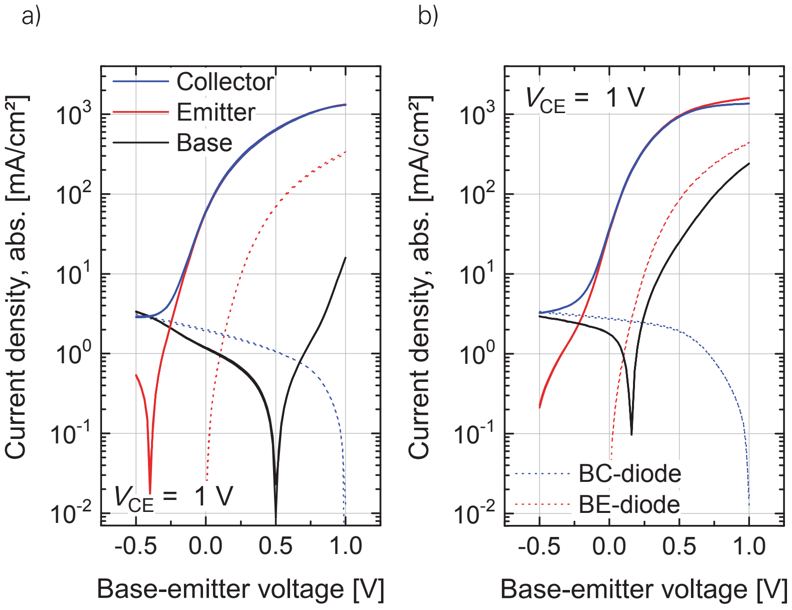

Figure 8.7: Base sweep at a driving voltage of 1 V using (a) the top electrode as emitter or (b) the bottom electrode as emitter. In both configurations, 1 A/cm^2 is reached in the on-state. For comparison, the currents of the respective emitter diode are shown in forward direction with respect to the emitter potential $V_E = 0$ V and the currents of the respective collector diode in backward direction with respect to the collector potential $V_C = 1$ V. On/Off ratios are limited to around 500 by the rather high currents of the BC diode.

channel length $L = 10\,\mu$m, channel width $W = 100\,\mu$m, and a charge carrier mobility of 1.5 cm^2/Vs reaches a transconductance of 15 µS at current of ca. 15 µA [110]. This would correspond to a transconductance of 10 mS at 10 mA, somewhat lower than realized by the VOT. The active area of such a corresponding OFET is 2 mm^2 if one takes the width of the source and drain contacts ($\Delta L = 10\,\mu$m, respectively) into account. By upscaling this OFET further to the active area of the VOT (4 mm^2), a transconductance of 20 mS could be achieved, so that the VOT is still better by a factor of 3 to 5. The additional advantage of the VOT is the much easier structuring if larger currents are needed.

The transmission values are highest if the top electrode is used as the emitter, reaching values of 99.84 %. This is also reflected in the large ratio between collector current and base current in the on-state region around a base-emitter voltage of 0.5 V to 1 V. Thus, differential current gains of up to 600 are realized at $V_{BE} = 0.3$ V. As a reason for this high value, it can be mentioned that besides a good alignment of the electrode, the on-state is reached at lower base-emitter voltages, eventually decreasing the leakage current from emitter to base through the native oxide layer. For comparison, the forward current of the emitter diode (BE) with the collector disconnected and the backward current of the collector diode (BC) with the emitter disconnected are plotted to their respective potentials in Fig. 8.7 as well. It is clearly visible that the emitter as well as the collector current density of the C_{60} triode is greater than the current density reached by the single BE diode, leading to a good current enhancement in the active area, still present in the on-state. Even at zero base potential, i.e. if no voltage is applied between base and emitter, charge carriers can be transmitted just by applying a voltage between collector and base.

Despite this promising performance of the VOTs, some challenges still remain. The on/off ratio remains rather low, reaching values around 500. Current densities in backward direction can vary over two orders of magnitude and thus on/off ratios between 10^2 and 10^4 have been measured for VOTs with equal or similar base-collector diode [181]. As a possible reason, a too small Schottky-barrier between the base electrode and the adjacent intrinsic C_{60} layers, as seen in Sec. 6.4 could be affected by slight variations of the fabrication. However, in all cases, the on-state can be clearly distinguished from the off-state, making it possible to discuss the physics of the VOT. Furthermore, due to the fabrication process and the alignment of the electrodes, the highest charge carrier transmission can vary even between different samples of the same fabrication run. The next section will provide solutions how to decouple the performance of the VOT from the alignment of the electrodes.

8.4 STRUCTURING THE ACTIVE AREA

As seen in the previous sections, misalignment deteriorates the VOT performance, and even a small current flow into the base reduces the current gain significantly. In this section, two methods are presented which do not prevent misalignment, but can decrease its negative influence to a minimum.

Concept The concepts presented in this section try to enhance the current flow in an area where all three electrodes overlap with respect to all other areas. This can be done in two ways. One can improve the injection of charge carriers at the emitter by inserting a laterally structured doped layer as visualized in Fig. 8.8a). Considering the typical misalignment of the setup, the location of the doped layer can be chosen to be safely in the normal active area. This area defined by the doped layer is called the structured active area. However, in all other areas, the current flow should be orders of magnitude smaller, which is realized by a rectifying contact between the metal of the emitter electrode and the intrinsic organic semiconductor. If the Schottky-barrier describing this rectifying contact is not sufficiently high to suppress the current flow, this method of direct structuring does not work well. Sometimes it might be helpful to exchange the metal electrode material to reach a lower injection in the non-structured active area while the doped layer in the structured active area still guarantees improved injection from the metal. A further advantage of direct structuring is that in integrated circuits, neighboring transistors do not share a doped layer which is likely to prevent crosstalk currents.

Unfortunately, C_{60} is one of the few organic semiconductors forming insufficient rectifying contacts to most metals. For example, reports on rectifying C_{60} diodes show currents in backward direction of the order of 1 mA/cm^2 or higher [253, 538] at voltages of 1 V. The C_{60} diodes used in this work employ the base electrode as the rectifying contact and show similar current densities but only if the aluminum is exposed to air. As a consequence, the achievable enhancement of the current density in the structured active area with respect to the residual area would be too low to detect high current gains so that the exclusive use of direct structuring for C_{60}triodes is not recommended. Nevertheless, an advantage of direct structuring is that the bidirectional oper-

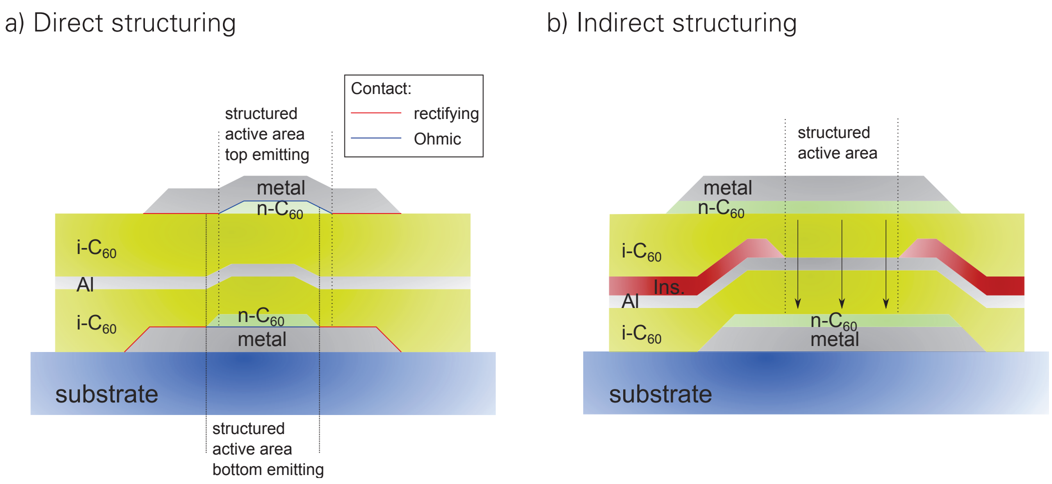

Figure 8.8: Schematic device cross-sections showing possible solutions to circumvent misalignment. a) Direct structuring. Doped layers realize an Ohmic injection in an area where all electrodes overlap. Outside this structured area, rectifying contacts between the outer electrodes to the intrinsic semiconductor ensure a reduced current flow. Both top or bottom electrode can be used as the emitter since charge carriers can leave the device at the opposite electrode (collector). Instead of a doped layer, different metals can be used to ensure Ohmic injection. b) Indirect structuring. A structured insulating layer limits the current flow to an area where all electrodes overlap. The structured layer is inserted above the base electrode if the top electrode is used as the emitter. In this case, using the bottom electrode as the emitter would result in a larger misalignment, since charges are not able to get transmitted in areas with an insulating layer.

ation is preserved since charge carriers can leave the device at the collector independently of the possible presence of a doped layer adjacent to the collector contact.

An alternative is indirect structuring. This method is independent of the combination of the organic semiconductor and the material of the metal electrode, because it introduces a structured insulating layer which suppresses the current flow in unwanted areas (cf. Fig. 8.8b)). As a consequence, current injected at the emitter can only reach the base and be transmitted where no insulating layer is present. Thus, a structured active area is realized which is definitely located where all three electrodes overlap. As insulating layer, typical inorganic insulators like silicon dioxide SiO_2 or aluminum oxide Al_2O_3 could be used so that this method allows to reach the highest current enhancement δ between the structured active area and the remaining area. However, by inserting an insulating layer between the emitter and the base electrodes, one has to decide which direction of operation is of interest. For the opposite operation direction, the insulating layer is then positioned between base and collector, preventing some of the transmitted charges to reach the collector and thus lowering the current gain. As mentioned above, direct structuring is problematic for VOTs using C_{60} due to the absence of appropriate rectifying contacts so that further optimization steps are carried out with indirect structuring using a structured insulating layer.

Shadow mask design All layers of the C_{60} triode are structured by thermal evaporation through shadow masks. For direct structuring, where the doped layers have to be defined, a mask with an opening in the middle of the requested area is appropriate. In contrast, for indirect structuring,

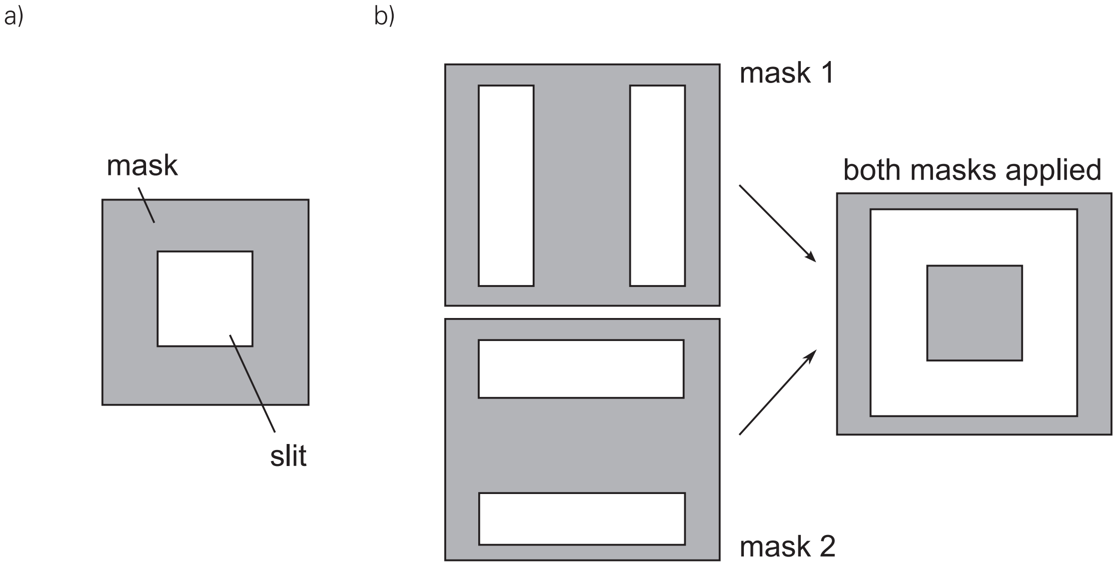

Figure 8.9: Shadow mask design for a) direct structuring to define the area of the doped layer or b) indirect structuring with two masks to define the area for the insulating layer. White areas will be covered with the material evaporated, gray areas remain free.

where exactly the opposite area has to be defined, it is not possible to use a single mask. Such a mask would require a freestanding part without connection to the rest of the mask defining the structured active area. This problem can be overcome by using two shadow masks instead of one. Fig. 8.9 shows the shadow mask design for direct and indirect structuring. For the latter one, the insulating layer must be deposited around the structured active area. A first mask realizes vertical stripes whereas a second mask realizes horizontal stripes of insulating layer next to the desired active area. Both masks applied subsequently finally lead to a structured insulating layer with an opening defining the structured active area. Besides the misalignment of emitter, base, and collector electrodes, the masks for direct or indirect structuring could also have a similar misalignment. However, by choosing a small active area with a sufficient spacing to the border of the region where all three electrodes overlap, it can be ensured that a mask misalignment does not lead to a device failure.

Insulating material Typically, one would use insulators like silicon dioxide or aluminum dioxide as insulating materials. Since the evaporation setup does not allow to deposit these materials, an alternative approach is used. Besides inorganic materials with high energy gaps, many organic materials also have rather large energy gaps in the range of 3 eV, giving the possibility to form high energy barriers for electrons at the organic/organic interface. Furthermore, these materials often have a low mobility, making them ideal to reduce the current flow in the structured non-active area. Typical materials are used in OLEDs as electron barrier layer or in OSCs as hole transport layers. The corresponding molecules have usually high HOMO levels and thus even higher LUMO levels around 3 eV below the vacuum level [539]. In contact with C_{60} (LUMO: $\sim$4.0 eV), the energy barrier between both materials could be in the range of 1 eV.

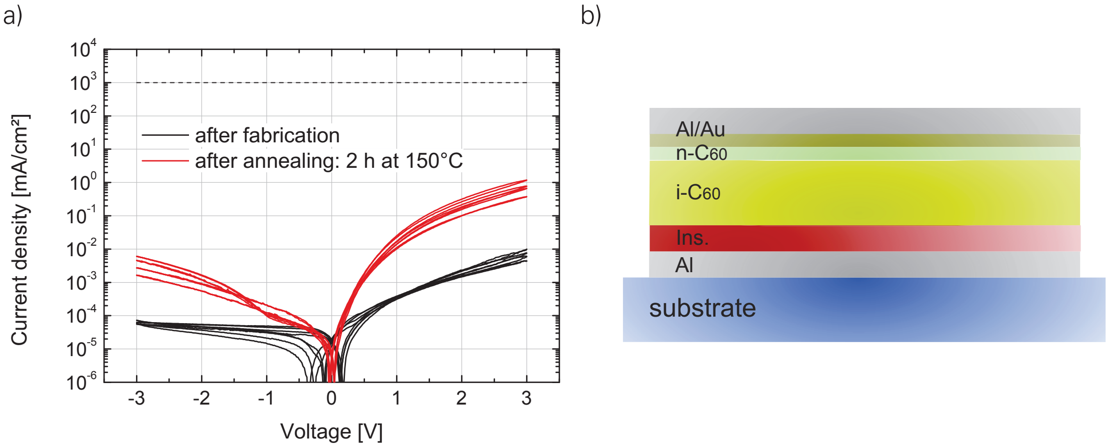

Figure 8.10: a) IV characteristics measured in forward and backward sweep of four devices shown in b) before and after annealing at 150 °C. All layers cover the active area (ca. 4 mm^2) of the two-terminal devices defined by the overlap of the two electrodes. The dashed line represents a current density of 1000 mA/cm^2 as reached in the on-state of the C_{60} triode, representing a reference value for the possible current enhancement in the structured active area with respect to the insulated region.

Several materials are tested and the best results are obtained for Spiro-m-TTB (Spiro-tetra(p-methyl-phenyl)-benzidine) [483]. In Fig. 8.10a), the IV characteristics are shown. Before annealing, the current densities do not exceed 10^{-2} mA/cm^2 in the applied voltage range. For comparison, the transmission current density reaches 1000 mA/cm^2 at similar voltages between emitter and base. Thus, by using Spiro-m-TTB as the insulating layer, the current density is reduced by 5 orders of magnitude, sufficient for the purposes of indirect structuring. However, C_{60} triodes are annealed to reach a high transmission factor so that the insulating layer must withstand the same treatment. After annealing, the current densities increase by two orders of magnitude for positive voltages (electron injection at the doped layer) still guaranteeing a current enhancement of three to four orders of magnitude. Calculations in Fig. 8.2 reveal that this would be sufficient to detect a current amplification of at least 100.

Sample setup The layer structure equals the one used for the samples in Sec. 5. The intrinsic layer thickness of the emitter and the collector is 100 nm, and adjacent to the top electrode, a doped layer is inserted in order to minimize the electron injection barrier. The layout of the electrodes can be seen in Fig. 8.11a). Four devices per sample with varying active area are realized which can be individually measured. The base electrode is enhanced in thickness outside the active area in order to minimize the series resistance and to ensure a proper conduction along the originally 15 nm thin electrode. Figure 8.11b) shows the mask setup for depositing the insulating layers. The first mask is used to evaporate 50 nm of Spiro-m-TTB above and below the desired active area, whereas the second mask is used to deposit the same material thickness to the left and to the right of the active area. Thus, there are some regions located in the direction of the corners of the structured active area where both insulating layers overlap and where the final thickness is 100 nm. The mask setup realizes different active area for each device of the sample so that the variation done by indirect structuring is highly comparable because all other layers are identical and have undergone the same treatment. Figure 8.11c) contains a camera picture of the

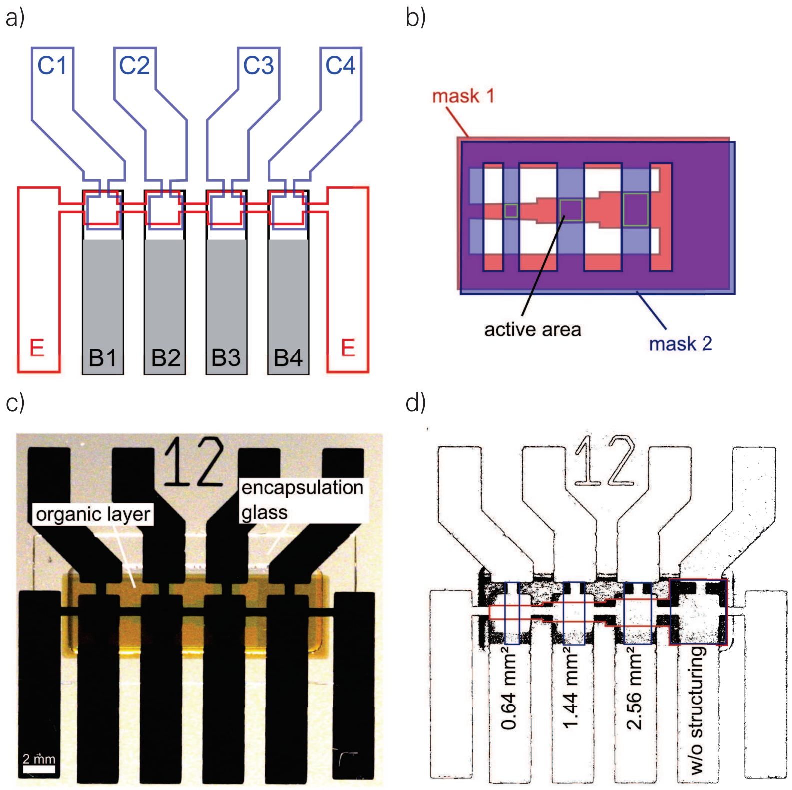

Figure 8.11: Sample setup for indirect structuring. a) Mask layout for the common emitter electrode (E), the four base electrodes (B) with grey areas, showing regions enhanced in thickness, and the four collector electrodes (C) so that four pixels per sample are realized. b) Mask layout to structure the insulating layers. With the help of mask 1, areas above and below the active area are insulated, whereas mask 2 structures the regions to the left and to the right of each pixel. c) Camera picture of the sample with four different pixels. d) The picture of c) is converted to black-and-white with adjusted brightness threshold levels to emphasize the insulating layers. The blue curve depicts the areas with no insulating layer defined by mask 1 and the red rectangles show the regions free of insulator defined by mask 2. It can be assumed that all structured areas are part of the area where all three electrodes of each pixel overlap.

finished device after encapsulation. Although the structured active area is not directly visible, the organic layer around the devices changes its color and brightness, depending on the presence of the insulating layer. By using a conversion to black-and-white and by choosing an appropriate threshold level, regions of insulating layers appear as fully black or white regions around the device area. A comparison with the mask design enables the identification of the layer positions as marked in Fig. 8.11d). Blue lined regions indicate the absence of insulator as defined by mask 1 whereas the red rectangles are regions free of insulator defined by mask 2. The cross section of all regions defines the structured active area where no insulating material is deposited, varying from 0.64 mm^2 over 1.44 mm^2 to 2.56 mm^2. It can be assumed that these areas are located within the area where all electrodes overlap. The last device is not structured and acts as the reference sample. Processing of the insulating layers is done after the base contact is finished and exposed to air. Finally, samples are encapsulated and annealed with the standard procedure at 150 °C for 2 h.

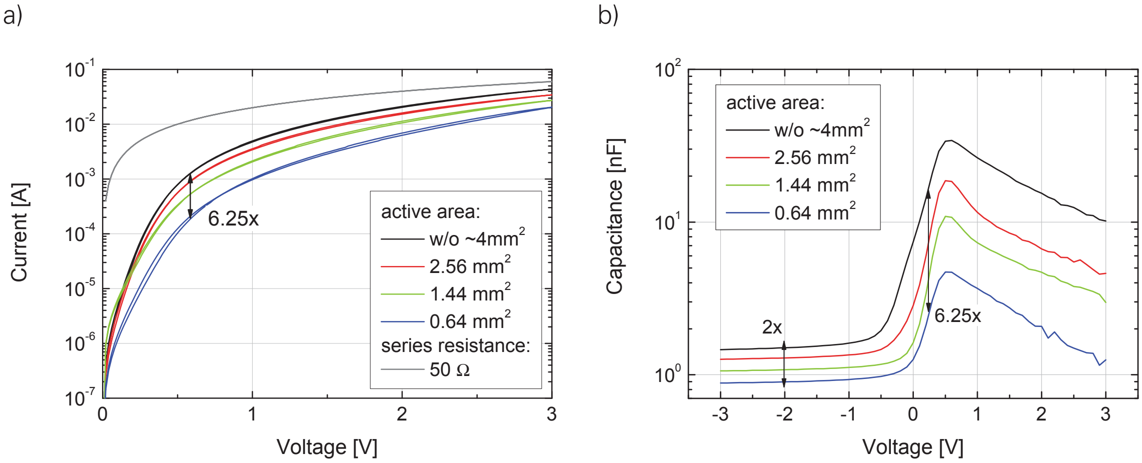

Figure 8.12: a) Current-voltage curves in forward direction of the top diode of the C_{60} triode as shown in Fig. 8.8. For a constant voltage, currents scale with the active area, defined by an insulating layer. However, at the highest currents, a limitation by a series resistance appears which is expected to be similar for all diodes. The curve for an active area of 1.44 mm^2 has a higher leakage current in parallel to the top diode, leading to a deviation at the lowest voltages. b) Capacitance-voltage measurements of the top diode of the C_{60} VOT (with disconnected bottom electrode) at a frequency of 1 kHz. At positive bias, charges accumulate in front of the native oxide of the base contact, and the highest capacitances are measured, scaling with the active area. In backward direction when the intrinsic layer depletes, the lowest capacitances are measured, and an additional capacitance reduction due to the insulating layers has a smaller influence.

IV and CV characteristics In order to prove the correct function of the insulating layers, IV characteristics of the top diode for different structured active areas are measured (cf. Fig. 8.8). Figure 8.12a) shows the result. For this measurement, the bottom electrode is disconnected and the current in forward direction is flowing from the top electrode directly into the base electrode, so that currents should scale with the structured active area. Indeed, from the curve with the smallest active area ($\sim$0.64 mm^2) and the curve with no structuring ($\sim$4 mm^2), the current changes by a factor of 6.25. Only at the highest currents, the curves converge as expected for a residual series resistance of the electrodes. For comparison, the current flow through a 50 Ω resistor is inserted into the diagram.

Furthermore, capacitance-voltage measurements can be used to show the influence of the passive structuring. As revealed in Sec. 7, the highest capacitances in forward direction are due to the accumulation of charge carriers in front of the base electrode. The corresponding capacitance is then given by the geometric capacitance of the thin native AlO_x layer. However, in regions where an insulating layer is deposited, the capacitance will decrease since this layer has a higher thickness and a lower permittivity. The capacitances of both regions, with and without insulating layer, are connected in parallel so that their sum gives the total capacitance. Since the capacitance of the aluminum oxide is much higher than that of the insulating layer, the total capacitance will be mainly governed by the oxide layer and should therefore scale with the structured active area. This behavior can be nicely seen in Fig. 8.12b) where the capacitance of the top diode depends on the active area and scales with the area variation exactly in the voltage regime (∼0.25 V) where the accumulation of charge carriers can be observed. At higher voltages, the capacitance drops due to the high leakage current through the aluminum oxide layer and the influence of the series resistance as explained in Sec. 7.3. Nevertheless, the variation of the capacitance with the active area remains visible. For comparison purposes, a factor of 6.25 is visualized in the diagram, corresponding to the ratio between the largest and the smallest active area. Only in backward direction, the variation is smaller than a factor of 2. This is not surprising if one assumes for the lower capacitance in the backward direction of the diode. In this direction the intrinsic layer is almost depleted, the total capacitance is rather given by the geometric capacitance of the 100 nm thick C_{60} thin film and partially the insulating layer. Consequently, the effect of an additional insulating layer with a thickness not higher than that of C_{60} cannot contribute more strongly than a factor of 2 between different structured active areas.

Thermal Imaging Besides electrical tests, the function of the indirect structuring can be proven by thermal imaging. For that reason, the VOT is kept in the on-state by externally connecting base and collector to the same potential. If the region of the current flow is defined by an insulating layer, the heat flow and the corresponding temperature rise must be in accordance with this structured area. Fig. 8.13 presents thermal images of two VOTs with different structured active areas. The three electrodes can be distinguished by their colors. For example, the top electrode appears as blue, the middle electrode red-orange and the bottom electrode is rather greenish. This variations can be explained by the thermal emission coefficient changing by region as they represent different stacks of layers and are also present if no voltage is applied. However, since thermal imaging is used here to depict he structures only, an absolute temperature calibration is not required. The dashed square shows the size of the designated active area and its position is chosen to be symmetrically aligned with the temperature rise, occurring in the top electrode (emitter) after applying a driving voltage. Indeed, the generated heat is located in the area where all three electrodes overlap and the size of the heated region is in accordance with the mask design of the indirect structuring. By varying the structured active area, the size of the heated region changes, corroborating the correct function of indirect structuring and justifying the comparison between differently structured transistors.

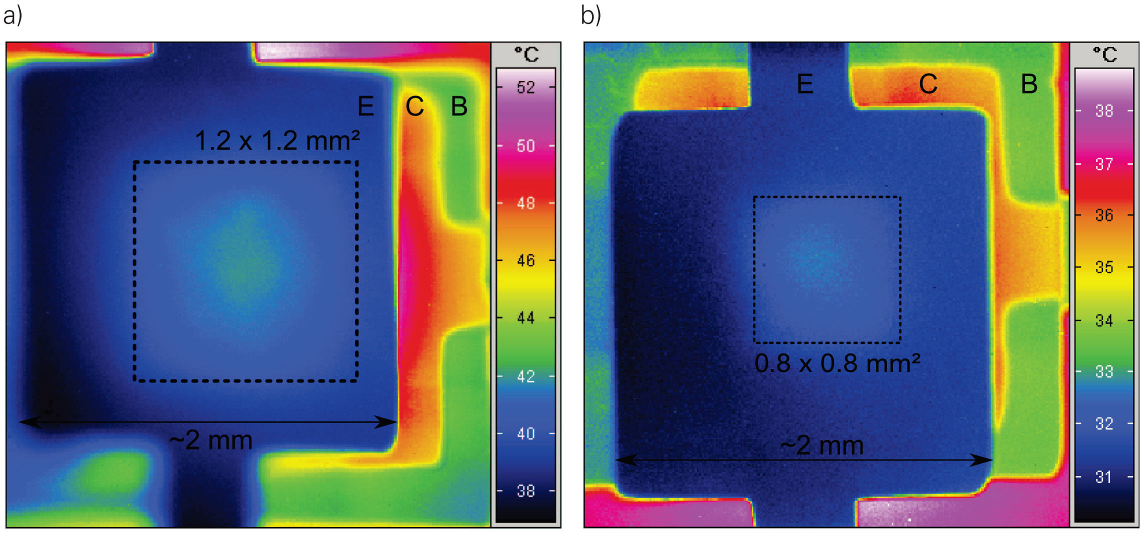

Figure 8.13: Thermal imaging of a device with an active area of a) 1.44 mm^2 (I = 57 mA, V_{CE} = 3.4 V) b) 0.64 mm^2 (I = 26 mA, V_{CE} = 3.7 V). Both devices show a temperature rise within the top electrode used as the emitter in accordance with the structured active area. The base is connected to the collector to ensure on-state operation by supplying power with a two-terminal Keithley SMU 2400. Electrodes are denoted with E (emitter), B (base), and C (collector), appearing in different colors due to a non-uniform emission coefficient. Since structural aspects are of interest, an exact calibration of the temperature is not done.

Transistor performance The performance of VOTs with and without indirect structuring is compared by using base sweeps at a driving voltage of 3 V. The result is presented in Fig. 8.14. In contrast to previous measurements, the y-axis depicts the collector current instead of the current density. Thus, it can be shown that although the currents of different devices vary at base-emitter voltages below 1 V, there is a limitation of the on-state current at 3 V for all devices. Only the VOT with an active area of 0.64 mm^2 has a 2-3 times smaller on-state current and therefore seems to be limited mainly by the transmission process itself. For all devices, the electrode resistance outside the device is similar and it is likely that the on-state performance of the VOTs with a larger active area is limited by a series resistance. For comparison, a dashed line in the diagram represents the current flow for series resistance of 30 Ω at a voltage of 3 V.

Figure 8.15 a) visualizes the respective current densities in the on-state as a function of the active area. The diagram clearly demonstrates a monotonous increase of current densities towards smaller active areas. Thus, record current densities above 5 A/cm^2 are realized at a low driving voltage of 3 V and from the trend of the curve, an increase of the current density seems to be possible by further reducing the active area. Besides that, the main achievement of indirect structuring is an improved current gain due to a decrease of current density in misaligned areas. Within the same figure, the maximum differential current gain is shown for various active areas. There is a distinct improvement between the reference device without indirect structuring and the device with the largest structured active area. The value of the current gain increases from about 100 to almost 600 just by inserting an insulating layer. The real strength of indirect structuring becomes obvious if the differential current gain is depicted vs. the actual collector current (cf. Fig 8.15 b)). The current gain does not only show an increased maximum, also the position of this maximum shifts to higher current, making it possible to now reach a high current gain in the on-state. Typ-

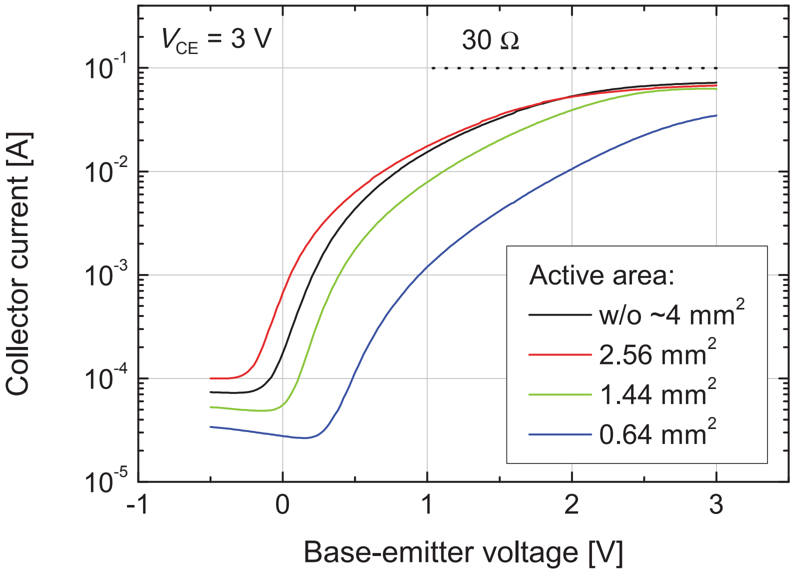

Figure 8.14: Base sweeps of a device without indirect structuring and indirect structuring of three different active areas. Structured sample show a decreased current with decreasing the active area.

ically, the current densities of the base-emitter diode can become quite high at a base-emitter voltage of 2-3 V. In this case, misaligned areas strongly contribute to the leakage current, flowing from emitter to base and reducing the current gain. The insulating layer is able to stop this current flow and thus it is revealed that the permeable base electrode of the VOT is capable to transmit high current densities without a loss in current gain. Nevertheless, indirectly structured devices with a small structured active area show a decrease of current gain. This fact is a strong hint for an insufficient quality of the insulating layer which shows a certain leakage current as reported in Fig. 8.10a). Especially, if the structured area shrinks, the alignment factor γ_E, defined as the ratio between the structured active area and the base-emitter electrode overlap, decreases and the base-emitter leakage current becomes more pronounced. In this work, an insulating layer made from small molecules has been used for reasons of easy fabrication and compatibility with the thermal evaporation setup. For further optimization of the indirect structuring, it is recommended to use insulating materials like oxides which have a lower leakage current density and a better thermal stability.

8.5 HIGH-FREQUENCY OPERATION

Approach Indirect structuring has several advantages for the performance of the device itself, but it is also interesting for integration of VOTs into more complex circuits. It is likely that applications like driving an OLED or selecting memory cells will need very small active areas to increase the device-per-area ratio. Typically, the feature size of these devices ranges from several 10 µm to 100 µm [540]. Without any elevated structuring methods, small misalignments of some µm can lead to drastic decreases in performance. Thus, it is probable that direct and indirect structuring will become an essential tool to fabricate arrays of VOTs on a large scale. Furthermore, devices that are usually limited by an external series resistance can reach higher switching speed if they

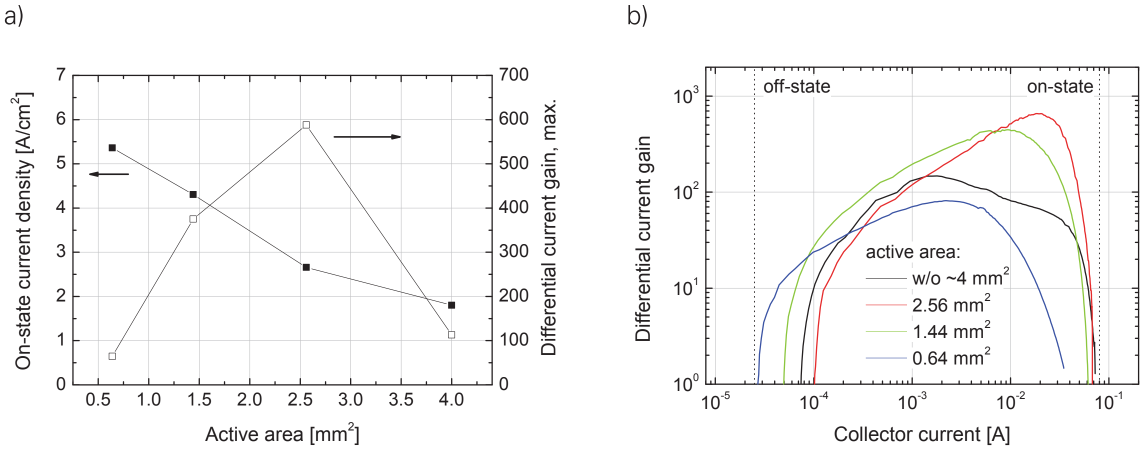

Figure 8.15: a) On-state current density and maximum differential current gain of a device without indirect structuring and three devices with indirect structuring. The smaller the active area gets the higher the current densities can become, pointing to a limitation by an external series resistance of the electrodes for devices with larger active area. The highest current gain is reached for a device with indirect structuring and a structured active area of 2.56 mm^2. Devices with a smaller active area have a lower differential current gain. Nevertheless, even a device with a structured active area of 1.44 mm^2 reaches a higher differential current gain than the reference device. b) Differential current gain of a VOT without indirect structuring (reference) and indirect structured active areas. By using insulating layers, it is possible to reach higher current gains in the on-state. However, if the active area gets to small, the differential current gain drops below the reference device, pointing to insufficient properties of the insulating layer.

have a smaller active area. Normally, the RC time does not depend on the active area, since the variation of device resistance and the device capacitance compensate each other. The situation changes when the series resistance limits the RC time of the device. By reducing the edge length of a quadratic active area, the series resistance of the electrode will only increase linearly with the edge length whereas the capacitance of the device decreases quadratically. Thus, a reduction of the active area allows to reach higher operation frequencies [56]. Finally, a drastically reduced active area could enable measurements of the upper limit of current densities which can be driven with a C_{60} triode since downscaled devices show an increased on-state current density.

For that purpose, a further set of shadow masks has been designed to reach an active area in the range of 200 µm × 200 µm. To keep the alignment factor as high as possible, the emitter, base, and collector masks are redesigned, having an electrode width of 600 µm. The overlap of all three electrodes is planned to be 600 µm × 600 µm with the structured active area in the center, so that even with a mask displacement of 200 µm, a working triode with an indirectly structured active area can be fabricated. Samples have the standard layer system introduced in Sec. 5, and they are annealed according to a procedure as discussed later in more detail. Due to their small active area and their capability to reach the highest operation frequencies, these device are further referred to as HF triodes.

Thermal imaging Before electrical tests are performed, the mask alignment of the sample is checked. Figure 8.16a) shows a thermal image of the HF triode at a current of 8 mA using a driving voltage of 3.2 V. The base is connected to the collector to realize on-state conditions

a) b)

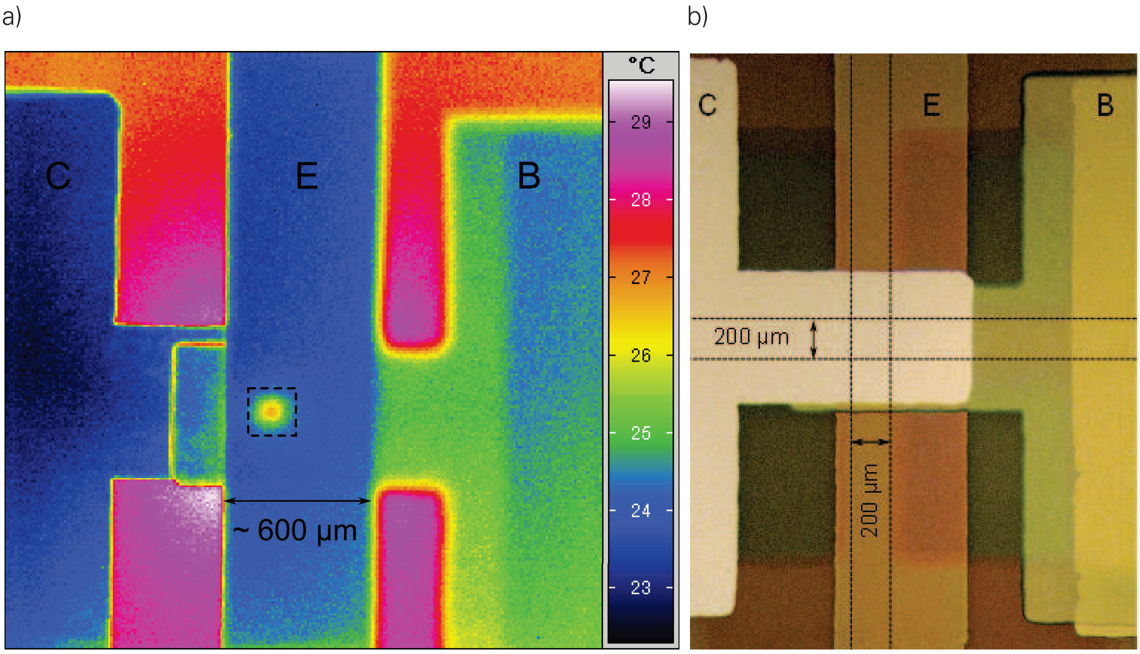

Figure 8.16: a) Thermal image of a VOT operating at 8 mA and 3.2 V taken through the encapsulation glass. The overlap of all three masks is around 600 µm × 600 µm. The inner dashed square has a size of 200 µm × 200 µm, in good agreement with the self-heated region of the VOT. b) Microscope picture of the HF triode through the substrate glass. The insulating layer changes the color appearance of the emitter (E) and the base (B) electrode. The collector (C) is in front of the layer stack and covers the indirectly structured active area. However, by the shape of the insulating layers outside the active area, it can be estimated that the structured active area has a size of 200 µm × 200 µm where all electrode overlap.

independently of the voltage applied between collector and emitter. The picture is taken through the encapsulation glass, looking onto the top electrode (E). With applied power, a temperature rise takes place within the area where all three electrodes overlap. The size of the heated region is in accordance with the indirectly structured active area of 200 µm × 200 µm. For comparison, an overlaid dashed square of this size is visualized.

To estimate the structured active area of the sample, pictures of the samples are taken with a microscope (cf. Fig 8.16b)). The direction of view is through the substrate glass which enhances the visibility of the insulating layers. These layers are visible along the emitter electrode (E) and along the base electrode (B) in the areas surrounding the active area. Since two masks are used to structure the insulating layer, stripes vertically and horizontally crossing the active area exist where only one layer of 50 nm Spiro-m-TTB is deposited, leading to a slight change in color. These regions are marked with dashed lines, and their cross-sections give the active area. The location of this area is in accordance with the region where the temperature rise appears in the thermal image, additionally proving the function of indirect structuring. Thus, the active area can be assumed to be 200 µm × 200 µm.

Annealing procedure Due to their small structured active area, the HF triodes have a very small alignment factor of around 10%. This means that most of the overlapping area between emitter and base is not used for the transmission process. Furthermore, the mask setup is designed in

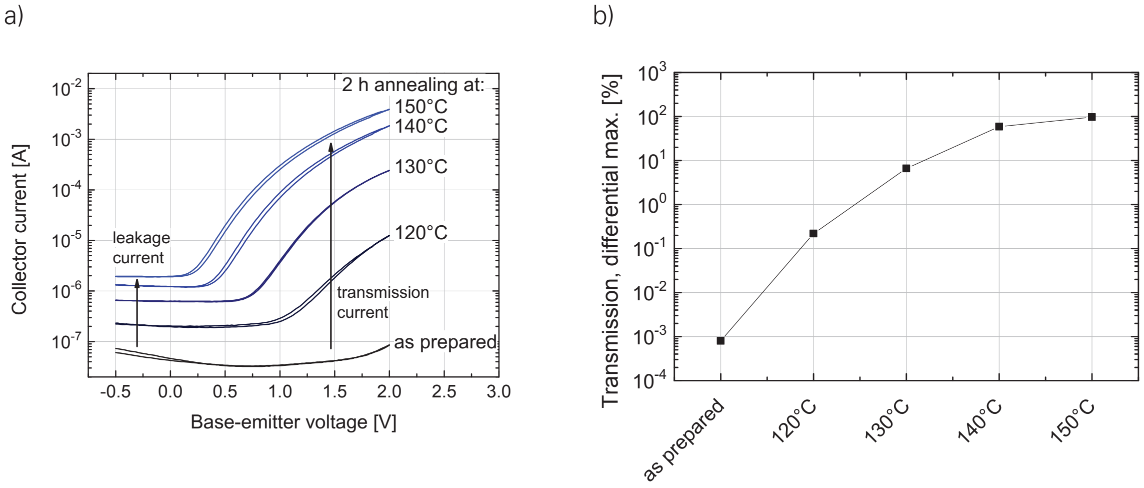

Figure 8.17: a) Annealing of one sample at different temperatures for 2 h. With increasing temperatures, the leakage current from emitter to collector increases, indicating a loss in quality of the insulating layer. b) Maximum differential transmission at different annealing temperatures. Although 120 °C are sufficient to reach a first increase in current gain, 150 °C are required to realize highest values which saturate around 100. All measurements are done after the sample has reached room temperature again.

a way allowing for an exclusive overlap of emitter and collector. The structured insulating layer, which is definitely present in those areas, circumvents the problem of uncontrolled current flow between emitter and collector. Nevertheless, the annealing procedure increases the leakage of the insulating layer as shown in this section. The consequences of the heat treatment are shown by annealing the samples for 2 h at several temperatures, increasing after each step.

Base sweeps at a driving voltage of 2 V are presented in Fig. 8.17. Directly after fabrication of the device, the increase of the collector current due to transmission is less pronounced at base-emitter voltages above 0.75 V. In the off-state at voltages below 0 V, the collector current is clearly below 10^{-7} A and varies with the base-emitter voltage, revealing that this current originates from backward currents through the base-collector diode. The first annealing step is done at 120 °C and leads to an increase of transmission current. Unfortunately, the current in the off-state increases as well. This behavior continues after repeating the annealing at 130 °C, 140 °C, and 150 °C for the same sample. The off-state current is now higher than 10^{-6} A and does not depend anymore on the base-emitter voltage. This plateau at low base-emitter voltage is a typical feature of leakage current flowing directly from emitter to collector in regions where the base electrode is missing. Due to the constant driving voltage, the corresponding leakage current also remains constant. Thus, the increase of the off-state current can be interpreted as a reduced quality of the insulating layer due to the annealing process. Nevertheless, the device has an on/off ratio of more than three orders of magnitude achieved by the huge increase of transmission current by more than four orders of magnitude, likewise as an effect of the annealing. Figure 8.17b) presents the maximum differential current gain after each step. Annealing at 150 °C finally leads to an increase by more than five orders of magnitude in comparison to the device as deposited, in accordance with previous results. The charge carrier transmission saturates close to 100 and annealing at higher temperatures is avoided in order to stop a further increase of the emitter-to-collector leakage current. Besides that, the most interesting fact is the high on-state current of

4 mA, implying that the current density of the transmitted current must be as high as 10 A/cm^2 if one uses the structured active area determined above. This is the highest value achieved for a fully organic vertical transistor compared to the literature presented in Sec. 3.2.

Base sweeps A base sweep measurement gives more detailed insight into the performance of the HF triodes for both operation directions. Figure 8.18 shows the result for a driving voltage of 2 V. If transmitted charge carriers are flowing into the direction of the substrate glass, using the top electrode as the emitter, a very good performance is achieved. The on/off ratio is as high as 1890, limited by a high leakage current from emitter to collector in the off-state. If this current could be suppressed, an enhancement by a factor 10 would become possible as it can be seen from the low base current in the off-state region. Furthermore, the current gain has a large value in the range of 100, even reached in the on-state as depicted by the ratio between collector current and base current. In this regime, the emitter and the collector currents are almost identical.

The situation changes if the bottom electrode is used as the emitter. While the method of indirect structuring only enhances one operation direction, it disturbs the performance for an oppositely directed current flow, since charge carriers transmitted through the base cannot reach the collector in regions, containing the insulating layer. Especially, if the alignment factor of one outer electrode is small, the transmittable current is strongly restricted when using the opposite electrode as emitter. In this case, most of the injected current at the emitter has to drop into the base electrode, leading to a drastically reduced transmission factor. This can be seen in Fig. 8.18b) where the bottom electrode is used as the emitter. In the on-state region, the collector current is only in the range of a tenth of the emitter current, in agreement with the alignment factor of the top electrode. Now, the emitter and the base current are almost identical. Only the leakage current in the off-state seems to be unchanged. It remains in the range below 1 µA due to the fact that the electrode overlap of emitter and collector is independent from the direction of the current.

Pulsed measurement Finally, to demonstrate the high-frequency operation of these small active area VOTs, pulsed measurements are performed at a constant driving voltage of 2 V similar to the base sweep[1]. A voltage pulse changes the potential at the base contact between 0 V (off-state) and 2 V (on-state), and the waveform of the collector and the base current is measured over time. The incoming pulse has a duration of 10 µs whereas the whole period has a duration of 20 µs. The slope of the signal has a rise and a fall time of 100 ns.

The waveform of the collector and the base current, shown in Fig. 8.19a), reveals that the modulated current signal is able to follow the incoming signal, but an oscillation occurs whenever a switching process takes place. This can be understood if one factors in the inductivity of the conducting paths. Together with the capacitance of the VOT, they realize an oscillation circuit which is able to modulate the signal whenever stimulated by an external change in potential. Nevertheless, the collector current exceeds 3 mA in the on-state and vanishes in the off-state, in

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[1] Measurements are done together with Stefan Slesazeck (Namlab gGmbH Dresden), using a Keithley Parameter Analyzer 4200-SCS equipped with a 4225-PMU Ultra Fast I-V Module

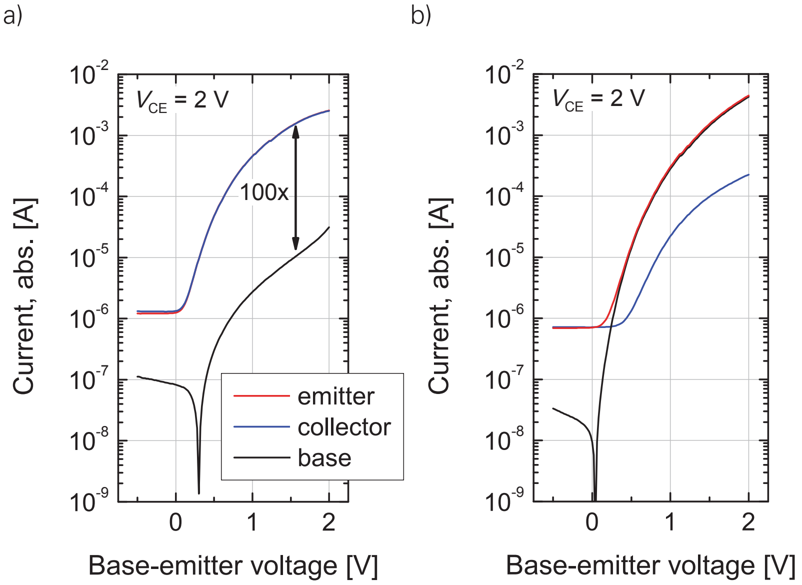

Figure 8.18: Base sweep measurement of a HF triode at a driving voltage of V_{CE} = 2 V for a) top electrode as emitter and b) bottom electrode as emitter. Due to the unidirectional operation enhancement of the insulating layer, transmission and current gain is enhanced for a) whereas for b) the current gain is disturbed. Please note that in a), emitter and collector currents are almost identical.

accordance with the base sweep measurement. At the same time, the base current is close to zero at all times excluding the switching process, showing the presence of a current gain. Figure 8.19b) and c) show zooms into a region where the voltage of the incoming signal is changed. The VOT needs 381 ns after the start of the voltage pulse to reach 90% of the final collector current. This rise time shortens to ca. 280 ns if the rise time of the incoming voltage pulse is taken into account. The switch off process is slightly slower and takes about 500 ns until 10% of the initial collector current is reached. A shortening of the rise and fall time of the incoming voltage pulse is prevented to keep the oscillations low.

To estimate the cutoff frequency of the VOT, a simple RC circuit can be assumed whereby the rise time of the measurement corresponds to a state in which the capacitor is charged up to 90% of its maximum value. One can show that the RC time is $\tau = (2\pi f_{\mathrm{c}})^{-1} = t_{\mathrm{rise}}/2.3$ and consequently, the cutoff frequency f_{c} is around 1×10^{6} Hz. Thus, the VOT reaches Megahertz operation at a low driving voltage of 2 V without any expensive structuring method. For comparison, Uno *et al.* show a similar device performance but use a Si-Wafer to build step-edge OFETs which excludes a possible flexibility of the devices [306]. There are several groups reporting higher cutoff frequencies, but the respective OFETs require driving voltages of 10 V or more [309, 541, 542]. An OFET with $f_{\mathrm{c}} = 2.2$ MHz is demonstrated by Ante *et al.*, working in a ring oscillator driven by a voltage of 4.2 V or less [115]. This device requires a high resolution stencil mask used to realize the required channel length of only 1 µm. Thus, although several groups have reached better cutoff frequencies, the strength of the VOT is the ability to drive very high currents at low driving voltages and reach high frequencies without expensive high resolution structuring methods.

Nevertheless, it is likely that there is still space for improvement. At the moment, a large part of the overlap between the emitter electrode and the base electrode is not used for the structured active area, but contributes as a parasitic capacitance. Employing a more precise mask aligner

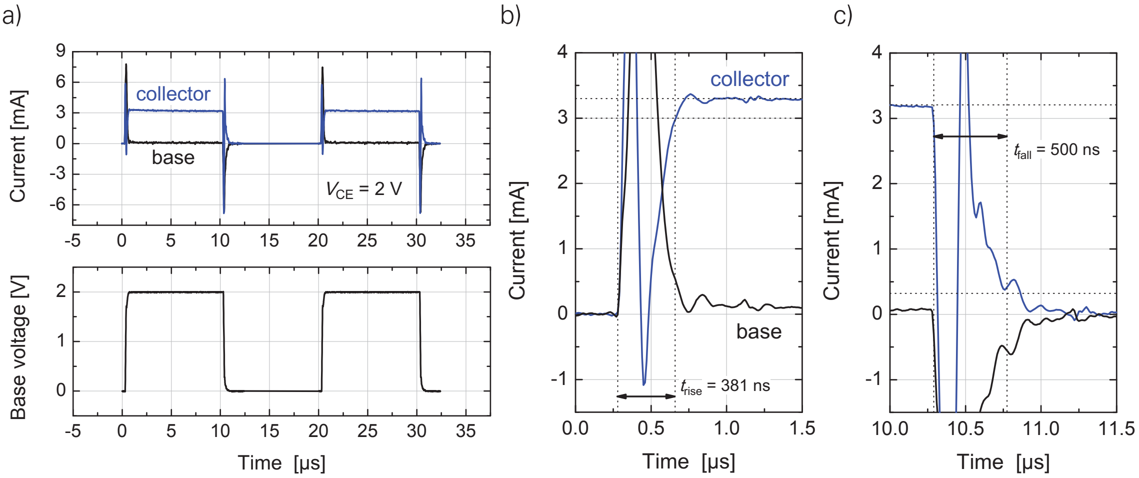

Figure 8.19: a) Pulsed measurement of a VOT with a downscaled active area of ca. 200 µm × 200 µm. The pulse has a width of 10 µs and the whole period lasts 20 µs. The fall and rise time of the voltage pulse is 100 ns. The signal of the collector current is able to follow incoming signal, but at the beginning of each switching process oscillations are visible which can be explained by circuit inductivities. b) After 381 ns, the collector current reaches 90% of its final value. c) The switch off process needs around 500 ns until the collector current falls to 10% of the starting value.

would allow to increase the alignment factor by decreasing the width of the electrodes, enabling faster RC times. Parasitic capacitances could also be decreased by a higher thickness of the insulating layer since the geometric capacitance of the layer decreases. Most important will be the design of an optimized contact layout with a minimized inductivity to prevent oscillations at the beginning of the switching. Then, it could be possible that a higher switching speed is revealed just by minimizing the influence of oscillation circuits onto the measurement.

8.6 INTERMEDIATE SUMMARY

In this chapter, several opportunities to optimize VOTs have been demonstrated. An essential step is the introduction of a doped layer into these devices. Similar to OLEDs, the contact resistance can be easily reduced just by inserting an additional layer. Higher current densities at low voltages are achieved and even the current gain increases as a consequence of the improved current enhancement in the active area which counteracts the misalignment of the electrodes. Two different solutions were presented in this section, allowing to solve the problem of misalignment. While direct structuring changes the extent of the doped layer, indirect structuring inserts an additional insulating layer to prevent the current flow in misaligned areas. With the help of the latter technique, VOTs reaching driving current densities up to 10 A/cm^2 at a driving voltage as low as 2 V have been built. These transistors show a current amplification larger than 100 up to the on-state, and the fast signal response corresponds to cutoff frequencies of 1 MHz.

However, these devices can still be further improved. At the present stage, current gains between 100 and 1000 are achieved, corresponding to transmission factors of 99% to 99.9%. Higher values require a better passivation of the native oxide, surrounding the base electrode.

For example, a controlled atmosphere of oxygen and water vapor could be used to vary the properties of the aluminum oxide during oxidation. A second major issue is the low on/off ratio of 3 to 4 orders of magnitude. There are two opportunities to address this problem. First, an improved quality of the native oxide around the base electrode will not only suppress the leakage current from emitter to base, but can also reduce the leakage from base to collector. Second, one could try to increase the Schottky-barrier between the intrinsic collector layer and the base electrode by modifying the interface. P-dopants and transition metal oxides could produce a charge transfer to the adjacent metal electrode due to their energetically deep lying energy levels, influencing the electron injection barrier. Nevertheless, it is mandatory to keep the leakage current between emitter and collector as low as possible by using indirect structuring with high quality insulating layers. Then, it could become realistic to reach on/off ratios up to 10^6. A further increase of the on/off ratio by enhancing the current density in the on-state is unlikely since $10\,\mathrm{A/cm^2}$ is already a remarkably high value. One has only to ensure that residual series resistances of the emitter and the collector electrode do not limit the device performance.

9 SELF-HEATING IN ORGANIC SEMICONDUCTORS

Vertical organic triodes comprising C_{60} have low driving voltages of only a few Volt. Nevertheless, since they have huge current densities, the dissipated power leads to a temperature rise of the device as shown in the previous section. For organic semiconductors, self-heating is a serious problem since they mostly have a low glass transition temperature in the range of 100 °C due to their weak van-der-Waals bonding [543]. As a consequence, the layer stack becomes unstable and short cuts as well as device failure can occur [544]. Furthermore, higher temperatures can lead to a chemical degradation of the material. Especially for OLEDs, self-heating is one of the main obstacles, inhibiting the realization of very large and bright lighting tiles [494].

Fortunately, the compounds used in C_{60} triodes are highly temperature stable. Both molecules, C_{60} and $W_2(hpp)_4$, do not decompose at temperature of at least 300 °C. If $W_2(hpp)_4$ is doped into C_{60}, these layers can be annealed at 150 °C even leading to an increase in conductivity, which is discussed in Sec. 6. Thus, self-heating up to a similar level of temperature is not expected to worsen the operation, making C_{60} devices ideal candidates for applications with elevated power consumption accompanied by a significant temperature rise.

Since the electrical resistance of a semiconductor typically depends on the temperature, an electrothermal feedback between the electrical circuit and the thermal circuits occurs. In the worst case, this leads to a positive feedback between the conductivity and the power dissipation, ultimately destroying the device by thermal runaway as outlined in Sec. 2.3 for an ideal NTC thermistor. For example, the effect has become a major problem for long-term reliable inorganic integrated circuits with sub-130 nm feature size. It limits the long-term stability, since the temperature-dependent leakage current strongly increases [545].

Here, possible influences of self-heating in organic semiconductors will be discussed. These materials are known to increase their conductivity with rising temperature, which can cause a positive feedback loop. First, the temperature dependence of C_{60} triodes is investigated to check whether these devices are principally prone to thermal runaway. Then, it is demonstrated that

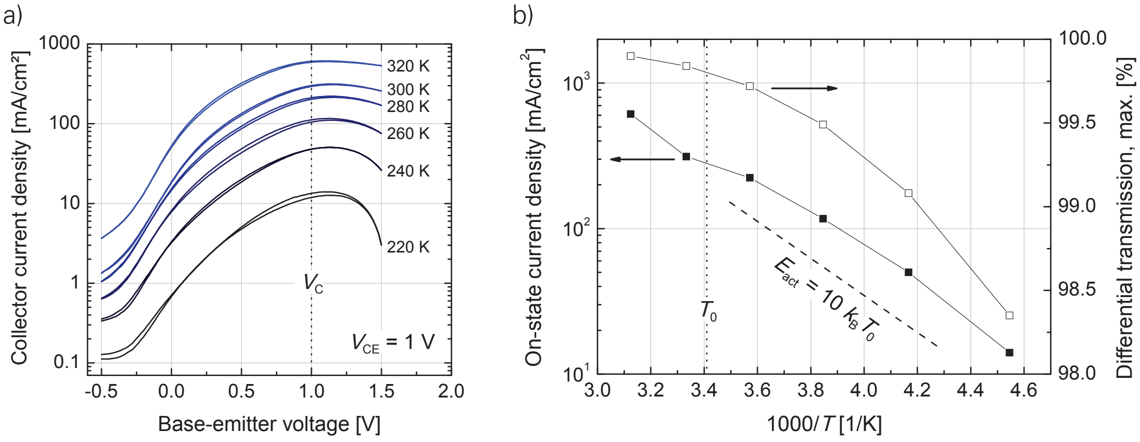

Figure 9.1: a) Base sweep measurement of a C_{60} triode with a driving voltage of 1 V measured with forward and backward sweep. Currents are monotonically increasing with rising temperature. However, at the highest temperatures, an influence of self-heating cannot be excluded which could lead to an additional rise of the on-state current. b) Temperature-dependent measurement of on-state current density and maximum differential transmission for a C_{60} triode. The dashed line is a guide to the eye for an activation energy of 10 $k_B T_0$.

organic semiconductors suffer from this particular problem, and it will be discussed how self-heating can be studied in crossbar architecture.

9.1 TEMPERATURE ACTIVATION IN C_{60} TRIODES

C_{60} triodes using the layer stack presented in Sec. 7 are used to investigate the temperature activation of the transmission current. The sample investigated has doped layers of 20 nm and intrinsic layers of 200 nm on both sides of the base electrode. Figure 9.1a) presents base sweeps at a driving voltage of 1 V for a temperature variation from 220 K to 320 K in steps of 20 K. It is clearly visible that the collector current is continuously increasing with rising temperatures. Thus, the transmission current through the base electrode, which can be seen in the on-state, is activated by temperature. In the off-state, the measured collector current is given by the injection of charge carriers at the base electrode flowing to the collector. As described by the theory of thermionic injection (cf. Sec. 2.2.2), this process is temperature activated, as usual if an energy barrier has to be overcome by charge carriers.

The activation energy of the conductivity plays a key role for the possible thermal runaway. A value higher than 4 $k_B T_0$ is a necessary prerequisite for thermal runaway due to self-heating as outlined in Sec. 2.3. In Fig. 9.1b), the on-state current density is plotted vs. the inverse temperature. The current density does not follow a strict Arrhenius-like law which would correspond to a straight line as indicated for an activation energy of 10 $k_B T_0$. This value is sufficiently high to realize thermal switching upon self-heating so that VOTs could basically suffer from an abrupt breakdown. Indeed, this has been observed for devices with a small active area which seems not to be limited by an external series resistance in their on-state. Then, during thermal imaging, it is possible to observe that these devices will strongly overheat if the voltage is in the range between 3 V to 4 V.

Besides the transmission current, the transmission factor itself increases with temperature as shown in Fig. 9.1b). For example, around room temperature T_0, a transmission factor of 99.8% is reached, whereas the highest value is obtained at 320 K with 99.9%, meaning that only one of every thousand electrons injected at the emitter drops into the base electrode. However, even at the lowest temperature, the maximum differential transmission still exceeds 98%. A less favorable behavior at low temperatures can be seen in Fig. 9.1a). For base-emitter voltages above the collector potential $V_C = 1$ V, the collector current drops. Although the current injected at the emitter rises with temperature, a non-vanishing collector current remains if a reversed voltage is applied between base and collector. The situation changes at lower temperatures where the transmitted current decreases more quickly at base-emitter voltages between 1 V and 1.5 V. As an explanation, it should be mentioned that charge carriers transmitted through the collector can only reach the collector in this potential configuration by diffusion currents. Due to the temperature activated charge transport, the mobility decreases at lower temperature and thereby the diffusion length of electrons in the C_{60} layer will be reduced, making it more difficult for them to overcome the opposite applied electric field between base and collector.

The temperature activation of both, the transmission current as well as the transmission factor itself is in agreement with the current model of the device function. As outlined in Sec. 7.4, the accumulation of charges in front of the base electrode is beneficial for the transmission process since an effective current flow towards the openings of the base electrode takes place. Further, the transmission through an opening is realized by drift as well as by diffusion currents which are governed by the charge carrier mobility of the semiconducting material. As a consequence, the typically obtained temperature activated mobility and thus conductivity for organic semiconductor supports the transmission process.

In principle, for C_{60} triodes, the temperature rise accompanied by self-heating could lead to an improved on-state current density and current gain due to the enhanced charge carrier transmission and transport. However, of course, one has to take care that no thermal runaway can occur. These results indicate that an uncontrolled feedback between conductivity and power dissipation in vertical organic triodes and other devices based on organic semiconductors is possible. Nevertheless, investigations addressing this issue are missing in the literature. Thus, it will be the aim of the next sections to study such effects in organic semiconducting materials and to explain their behavior when used in a setup of crossbar electrodes, e.g. as commonly used for OLEDs.

9.2 NIN-C_{60} CROSSBAR STRUCTURES

To investigate possible influences of electrothermal feedback in organic semiconductors, a two-terminal device is used. In contrast to transistor devices, one bias is sufficient to operate the device, making it much easier to compare results with analytical expressions. Furthermore, the active area is reduced, enabling a simplified description of the heat transport. Nevertheless, the

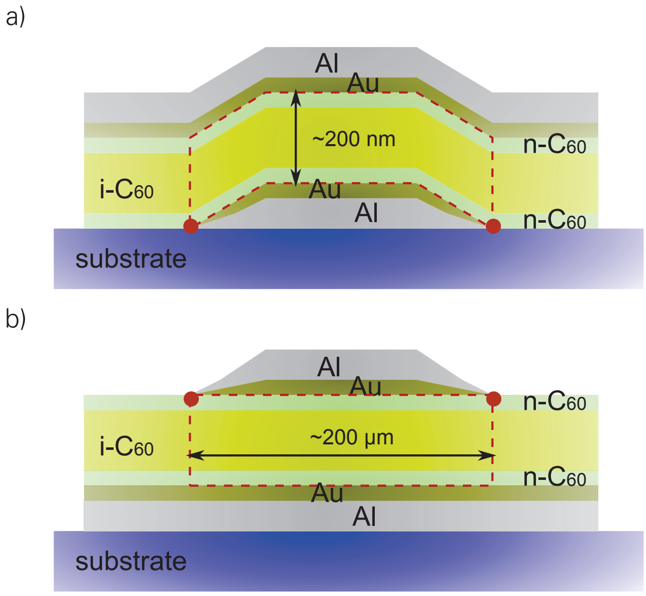

Figure 9.2: Layer structure of the nin-C_{60} crossbar devices. The pictures show the cross section midway through the a) top or the b) bottom electrode. The red dashed lines represent the volume in which homogenous Joule heating is assumed whereas the red points represent line heating along the edges of the electrodes near the active area. Arrows show the typical dimensions of the sample, demonstrating the large aspect ratio.

following results should also be applicable for C_{60} triodes as long as the base potential guarantees on-state conditions[1].

Experimental A suitable test structure requires an organic material with a sufficiently large conductivity, an activation energy $E_\mathrm{act} > 4\,k_\mathrm{B}T_0$, thermal stability up to rather high temperatures, and negligible influence of injection barriers. All these requirements are perfectly met by nin-C_{60} crossbar structures grown on glass substrates, employing n-doped C_{60} (n-C_{60}) layers adjacent to the metallic contacts, an intrinsic layer (i-C_{60}) in between, and a relatively small active area of about 0.06 mm^2. Figure 9.2 visualizes the sample setup employing crossbar electrodes. The thickness of the central intrinsic layer is varied from 100 nm to 400 nm, with the thicknesses of the n-doped layers kept fixed at 20 nm. The resulting sequence of layers is embedded between two metal electrodes using a combination of Al (>200 nm) and Au (20 nm). Thus, the aspect ratio between the width and the thickness of the device is in the range of 1000:1, large enough to expect a homogeneous current flow in the device.

C_{60} as n-type organic semiconductor with a mobility up to 0.5 cm^2/Vs ensures high current densities at moderate driving voltages [253, 394]. Doping of C_{60} is realized by co-evaporation with tungsten paddlewheel $W_2(hpp)_4$ at a doping concentration of 2wt% [380, 523], guaranteeing Ohmic injection [51]. Structuring of the device is done by shadow masks, leading to electrodes of a typical trapezoidal shape [546] as schematically visualized in Fig. 9.2. Further details can be found in Ref. [318]. Such devices using a doped / intrinsic / doped layer configuration are ideal to investigate the charge transport of the material in the intrinsic region since the injection re-

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[1] The work presented in this section is partly published in Refs. [318, 437].

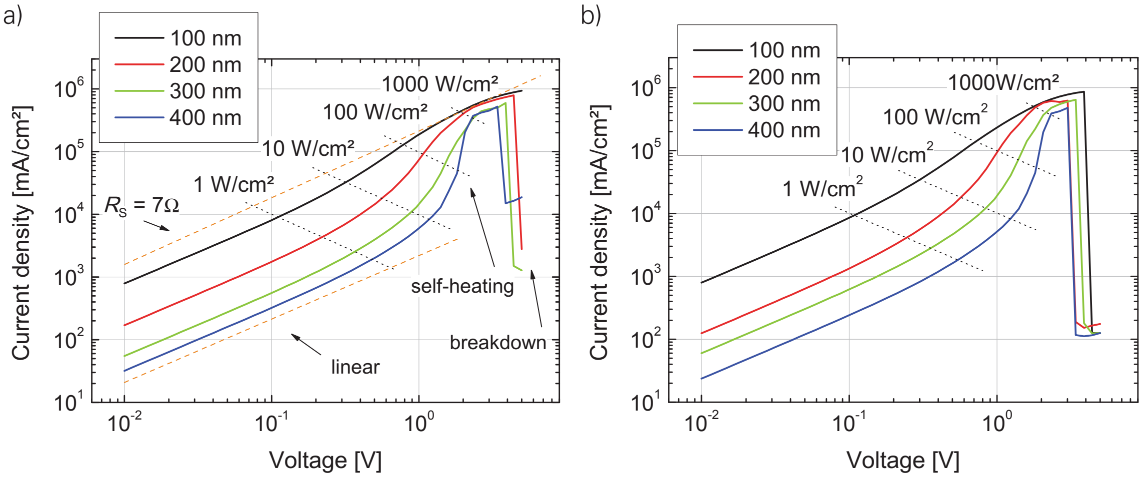

Figure 9.3: IV characteristics for different intrinsic layer thicknesses for electron injection at a) the top electrode and b) the bottom electrode.

sistance can be neglected [106]. Here, they fulfill a further purpose. Their structure coincides with C_{60} triodes except for the middle base electrode and that they have not been exposed to air. Thus, the achieved current densities can be seen as a limit for the maximum on-state current densities in C_{60} triodes.

IV characteristics The IV curves of the devices are shown in Fig. 9.3 for both directions, electron injection at the top electrode (a) or the bottom electrode (b). First, a symmetric device function is revealed. In the voltage regime below 0.5 V, irrespective of device thickness, the current-voltage dependence remains linear so that a non-Ohmic injection behavior can be excluded. Then, the conductivity of the sample is given by the charge carrier mobility of C_{60} and the residual charge carrier density in the intrinsic region, realized by charge carrier diffusion from the doped layers. At voltages beyond 0.5 V, a strong increase of current can be measured, especially for samples with large thickness of the intrinsic layer. One reason is that with increasing potential, space charges are formed in the device, leading to a superlinear IV characteristic (cf. Sec. 2.1.4). Drift-diffusion simulations of an nin device are discussed in the Appendix section A.5. Up to 1 V, such effects might explain why the IV curve leaves the linear regime. But at higher voltages, a strong rise of the currents occurs which is most distinct for device with a high intrinsic layer thickness. Then, the highest current densities reach 10^6 mA/cm^2, but still remain far below the highest published values for organic semiconductors [547]. The sharp increase in current is assigned to Joule self-heating, which is supported by thermal imaging discussed below. In Fig. 9.3a), additional lines of constant power density further suggest a correlation between the heating power and the IV characteristic: more than the voltage, the power density gives a threshold between constant temperature and the self-heating regime, starting at about 10 W/cm^2. A positive feedback loop between conductivity and power dissipation is initiated as described in Sec. 2.3 so that currents can show an accelerated increase with rising voltage. Consequently, nin-C_{60} crossbar devices seem to be suitable candidates for further investigations of thermal runaway in organic semiconductors.

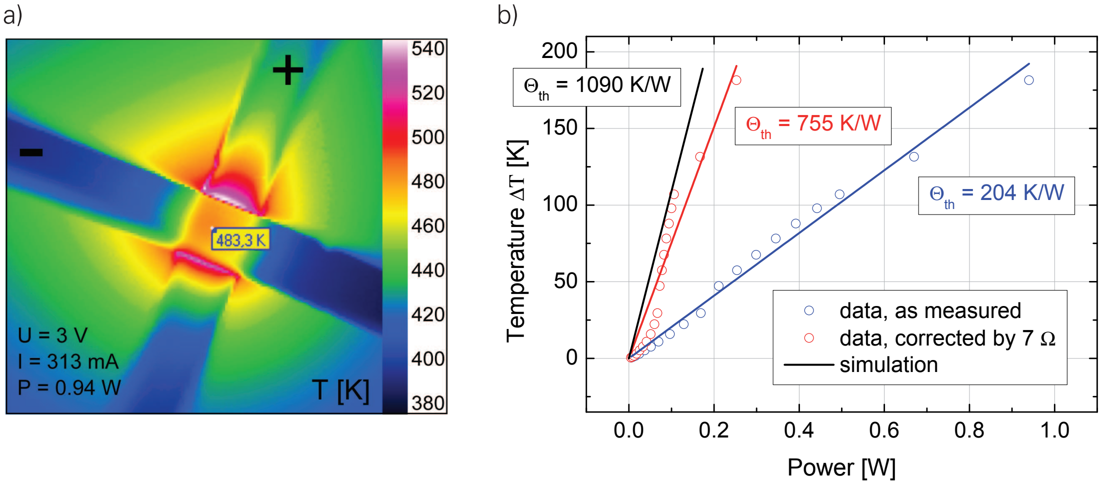

Figure 9.4: a) Thermal image of an nin-C_{60} crossbar device at 3 V, operating close to the thermal breakdown. The device reaches a temperature of around 483 K (210 °C) in the center of the active area. b) Determination of the thermal resistance by comparing the temperature rise for different applied powers. A series resistance of 7 Ω has to be considered, leading to an increase of the thermal resistance from 204 K/W to 755 K/W. A heat transport simulation as carried out in Ref. [318] reveals a value of 1090 K/W, in the same range as the fit to the experiment, corrected for the series resistance.

Since the thickest device with an intrinsic layer of 400 nm has the highest resistance at the beginning, the current rise starts at a higher voltage, but with a much steeper increase. Assuming a power law $j \propto V^{\alpha}$, an exponent of $\alpha > 10$ has to be used, in contrast to a device with 200 nm intrinsic layer thickness where $\alpha \sim 4$ is sufficient to describe the data. Around 3 V, all devices show a similar resistance which does not depend on the thickness of the intrinsic region. This results again in a linear behavior as expected for a limitation by a series resistance. In this region, the thinnest samples allow to assign a value of about 7 Ω to the series resistance. Finally, as shown in Fig. 9.3, thermal breakdown of the devices appears between 3 V and 5 V. In the device with 400 nm of i-C_{60}, the IV characteristic shows a collapse at slightly lower voltage, assigned to the fact that a thicker device has a higher temperature rise due to self-heating to reduce its resistance to a value of the order of the series resistance. For further experiments and simulations discussed in this section, a device with a 300 nm i-C_{60} layer is used.

Thermal imaging The following experiments are performed to show the temperature distribution in the device, produced by self-heating and to determine the thermal resistance required for analytical calculations. The temperature calibration is done by mounting the sample into a copper block heated externally. A slit ensures the visibility of the active area by the IR camera and two temperature sensors above and underneath the sample allow to measure the device temperature. The emissivity parameter is calibrated to 0.85 to adjust both measured temperatures for Al, resulting in systematic deviations in regions not covered by the contacts. Figure 9.4a) shows an infrared picture of an nin-C_{60} crossbar device exhibiting self-heating at a voltage of 3 V. At voltages shortly before thermal breakdown, the sample reaches temperatures of 483 K (210 °C) in the center of the device, demonstrating the astonishing high stability of C_{60}, making this material an excellent candidate for high power applications [253]. The edges along the top contact show an even higher temperature of 543 K (270 °C), in contrast to an expected homogeneous heat dissipation within the active area. Detailed simulations of the heat flow have shown that additional line heat sources have to be assumed along the edges of the electrodes around the active area to reproduce the experimental findings [318]. These line heat sources are visualized in Fig. 9.2 as red dots and are present at the edges of both electrodes along the active area. Although this result points to the fact that the current density in the device is not homogeneous, even if no self-heating occurs, it leads to more homogeneous temperature distribution within the active area. As a consequence, a one-dimensional description of the heat transport can be justified. Therefore, the further focus lies on the thermal resistance Θ_{th}

$$\Theta_{\mathrm{th}} = \frac{\Delta T}{\dot{Q}} = \frac{T_{\mathrm{ref}} - T_0}{\dot{Q}}, \tag{9.1}$$

since it will be needed in the analytical solution of the thermistor problem discussed below. It is a property of the complete device consisting of electrical circuit, substrate, and encapsulation glass, characterizing the temperature rise ΔT at a specific point within the electrically active region with respect to the room temperature T_0. In this case, the central point of the active area is used to compare the temperature rise for different applied powers as shown in Fig. 9.4b). The fit of the experimental data gives a thermal resistance of $\Theta_{\mathrm{th}} = 204\,\mathrm{K/W}$ for the entire circuit. However, the heating of the organic material reduces its resistance to a value below the series resistance so that the voltage drop across the organic layer decreases. Therefore, the part of the voltage dropping over the series resistor is subtracted and the recalculated data can be fitted to a value of $\Theta_{\mathrm{th}} = 755\,\mathrm{K/W}$. This value is in better agreement with the result of the heat flow simulation, $\Theta_{\mathrm{th}} = 1090\,\mathrm{K/W}$, obtained in Ref. [318]. The fact that a substantial part of the applied power already dissipates at the electrode outside the device can also be seen in Fig. 9.4a): The upper region lying between the electrodes with the applied potential (marked as '-' and '+') shows a higher temperature rise than other regions outside the active area.

Activation energy The activation energy of the conductivity in nin-C_{60} crossbar devices is measured by varying the ambient temperature from 200 K to 300 K in 10 K steps. In these measurements, the voltage sweeps from 0 V to 1 V are measured with a time step of 2 ms in order to avoid self-heating. Assuming that injection resistances are negligible due to doped layers next to the electrodes, the temperature activation of processes like charge transport in C_{60} are dominating. Besides that, charge transfer processes between dopant and matrix molecules can take place which also show a temperature activation [380]. At very low voltages in the linear regime, both effects contribute to the conductivity, whereas at higher voltages, space charges formed in the device reach a charge density due to charge injection comparable to the amount released by the dopants [58]. Then, injected charge carriers increasingly contribute to the overall conductivity and the temperature activation of the charge transport will dominate, especially in the intrinsic region. Please, consult Appendix A.5 for further details. At very low voltages (0.01 V), the highest activation energy of $\sim 9\,k_{\mathrm{B}}T_0$ is measured, dropping to $8.2\,k_{\mathrm{B}}T_0$ if the voltage is increased to 1 V (cf. Fig. 9.5). In this voltage range slightly above 1 V, self-heating occurs in nin-C_{60} crossbar devices, indicating that this value is sufficiently large to allow for thermal switching. The decrease of the activation energy could be explained by a lower contribution of dopant activation at higher voltage and by an increasing charge carrier concentration. Hence, electrons will reach higher

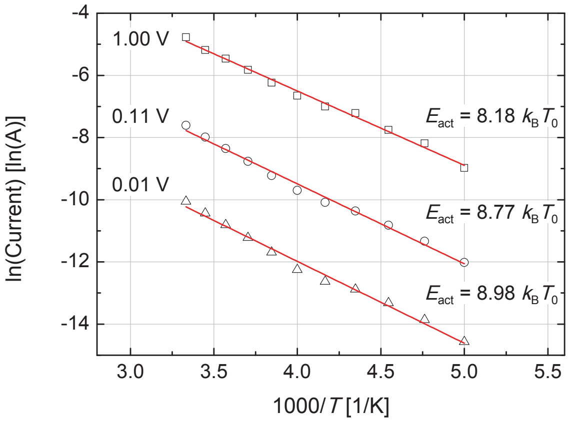

Figure 9.5: Activation energies of an nin-C_{60} crossbar device for different applied voltages. In the voltage range where self-heating occurs (1 V), the activation energy is 8.2 $k_B T_0$, sufficiently high for thermal switching. To avoid self-heating, every voltage step is applied for only 2 ms.

states in the Gaussian DOS, leading to smaller average energy barriers for a hopping event and thus to a smaller activation energy. However, the activation energy is a feature of the whole device, comprising both doped and intrinsic C_{60} layers so that an exact correlation between one of these effects and the measurement is not yet possible. The value is in the same range as in recent studies of the charge carrier mobility of C_{60} OFETs covering four orders of magnitude in charge carrier densities [359], and it also corresponds to the activation energy in the range of 10 $k_B T_0$ determined for C_{60} triodes in the Sec. 9.1. Due to this similarity, it is likely that the temperature activation of the transmission current in C_{60} triodes is governed by the charge transport in C_{60}, additionally influenced by the special geometry of VOTs. Please refer to Sec. 7.4 for further details.

9.3 THERMAL SWITCHING IN ORGANIC SEMICONDUCTORS

The previous section already indicated that nin-C_{60} crossbar devices show a drastically increased conductivity due to self-heating. As shown below, self-heating does not solely lead to a higher conductivity, but it is also responsible for a current regime in which the device shows negative differential resistance (NDR) [99]. Under constant driving voltages, this would mean that above a certain turnover voltage, there is no current matching the self-consistent description of the problem as outlined in Sec. 2.3. In consequence, a thermal runaway occurs, triggering switching from a less conductive state to a highly conductive state. If the device is not destroyed during that process, it is still able to switch down to the lower branch if the dissipated power becomes too low to ensure operation on the upper branch. This will happen at a second turnover voltage below the first turnover voltage. The presence of reversible thermal switching is a clear proof for the presence of NDR due to self-heating[2].

The direct observation of thermal switching requires a well-defined setup. First and most importantly, the activation energy of the device must be sufficiently high. Second, the highest

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[2] The work presented in this sections is published in Ref. [437]

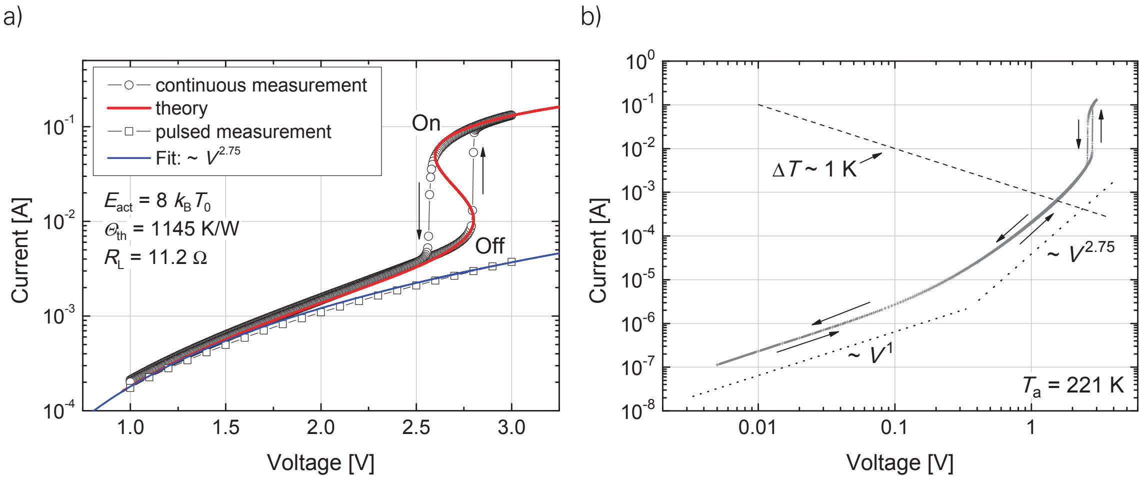

Figure 9.6: a) Thermal switching of an nin-C_{60} crossbar device at an ambient temperature of $T_a = 221$ K. b) Diagram, showing the full sweep. The dashed line indicates a temperature rise of 1 K, considering a thermal resistance of 1000 K/W. Shortly before substantial self-heating occurs, the IV curve follows a $V^{2.75}$ power law used in order to describe the isothermal behavior of the device in a).

temperatures achieved should not destroy the device so that materials with high temperature stability are preferred. For that reason, the series resistance to the device must be sufficiently high to prevent extreme overheating but still remaining low enough to enable thermal runaway. Thermal breakdown can be further prevented by cooling the device so that the temperature after thermal switching still remains acceptable. Third, the voltage required to reach sufficient Joule heating should not lead to electrical breakdown so that a high thermal resistance of the system is convenient. All these requirements are met by nin-C_{60} crossbar devices which are ideal to realize hysteresis loops with large height and width, without damaging the device by thermal runaway.

For the measurement, the ambient temperature is reduced to $T_a = 221$ K using a Peltier cryostat. Thus, even after thermal switching, the temperature remains sufficiently low to avoid thermal breakdown. The resistance of the electrodes and the measurement setup is about $7\,\Omega$ (c. Sec. 9.2) and is increased by an additional series resistor of $5\,\Omega$. The current-voltage characteristics in Fig. 9.6 are measured in a voltage sweep from 0 V to 3 V and back, with voltage steps of 5 mV held for time intervals of 0.15 s using a Keithley SMU 2400. At a voltage of 2.80 V, the circuit switches from the low conductivity OFF state to the high conductivity ON state. As long as sufficiently large voltages are applied, the system stays on the upper branch, but at 2.57 V it switches back to the OFF state, with a pronounced hysteresis between the two switching voltages. The thermal character of the switching becomes obvious in Fig. 9.6 when comparing to a measurement with short voltage pulses (Keithley 2635A, pulse width: 200 µs, repetition time: 200 ms). In this measurement, the curve can simply be described by a power law with an exponent $\alpha = 2.75$, $V_{ref} = 23$ V and $I_{ref} = 1$ A in Eq. (2.78), without any sign of an increase in sample temperature.

The theoretical approach outlined in Sec. 2.3 can be used to assign the key parameters of our device. Applying Eqs. (2.81) and (2.82) together with a load resistance R_L, one obtains the best agreement between measured and calculated current-voltage characteristics when assuming an activation energy of $E_{act} = 8\,k_B T_0 = 10.6\,k_B T_a$, in accordance with the value obtained for a fixed value of $V = 1\,\mathrm{V}$, a load resistance of $R_\mathrm{L} = 11.2\,\Omega$, and a thermal resistance of $\Theta_\mathrm{th} = 1145$ K/W, see Fig. 9.6. The thermal resistance is in the same range as the value of about 1000 K/W obtained by simulations of the heat flow [318]. The fitting procedure demonstrates that the bistability is a natural consequence of the thermally activated conductivity in the organic electronic circuit. Residual deviations between theory and measurement in the ON state at a voltage about 2.6 V may be due to the assumption of homogeneous steady state. After switching back to the OFF state, the voltage sweep downwards reproduces the previous sweep upwards, indicating that the device has not been damaged by passing through the entire hysteresis loop. A possible influence of a phase change in crystalline C_{60} at 251 K on the thermal switching can be excluded because such a phase change would decrease the conductivity by a small amount instead of increasing it by one order of magnitude [349, 354]. Changes of charge carrier concentration due to impact ionization at high electric fields can be neglected since they cannot contribute significantly at voltages below 3 V [548]. When present, they would also be observed in the measurement with short pulses. Consequently, the conductivity switching can be completely explained by purely thermal effects, revealing that nin-C_{60} devices constitute an interesting model system for further studies of thermally induced bistability. Furthermore, the observation of thermal switching induces that the device enters into a current regime with S-NDR [437] which will be discussed in more detail in the next section.

9.4 SELF-HEATING IN LARGE AREA DEVICES: ORGANIC LEDS

The measurements discussed in Sec. 9.3 show the presence of thermal switching in organic semiconductors. The analytical model describing the effect is zero-dimensional, meaning that the current distribution in the device is assumed to be homogeneous. This simplification is realistic because the width of the active area is smaller than the substrate thickness and thus the lateral heat conduction is able to realize a similar temperature rise in the whole device. Furthermore, both electrodes have a low sheet resistance so that the potential drop within the electrodes remains small and across the active area, similar voltages are applied.

The situation changes if the lateral dimension of the crossbar device becomes larger than the substrate thickness and if at least one of the electrodes exhibits a higher sheet resistance. These properties are typically met by OLEDs which can be fabricated on large areas and use transparent electrodes with non-negligible resistance. It is also known that these devices suffer on self-heating [490, 549–558]. Therefore, OLEDs are fabricated to study the occurrence of thermistor-like behavior in crossbar devices.[3]

4-wire crossbar setup For measuring possible NDR effects due to self-heating, a new measurement setup, called 4-wire crossbar, is created [475]. Figure 9.7d) visualizes this setup of an OLED crossbar structure as seen from the top. In a usual current-voltage measurement, the two different electrodes are contacted from a single side to apply a low ($V-$) and a high ($V+$) potential. The total current I flows between these potentials as realized by a current source. However, since

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[3] The work presented in this sections is published in Ref. [494].

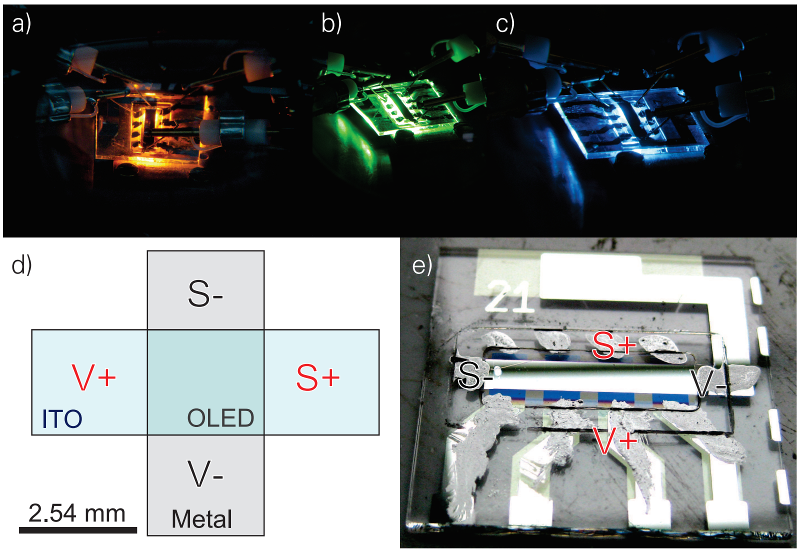

Figure 9.7: a)- c) Pictures of a red, green, and blue OLED during 4-wire crossbar measurement. d) Setup of the 4-wire crossbar measurement. The external voltage V is applied between $V+$ and $V-$. The contacts $S+$ and $S-$ are used to detect the voltage S at the backside of the device. e) Decapsulated sample after measurement. Silver paint covers the contacts to minimize residual contact resistances.

the electrodes overlap the active area, a second contact can be connected to each electrode to sense the potential present at the opposite side. For each electrode, independently whether the potential is low ($S-$) or high ($S+$), a sensing contact will be applied. The voltage S between both sensing contacts can be measured and compared to the originally applied voltage V between $V-$ and $V+$. The idea of this setup is that whenever a NDR will appear in the device, problems arising in two-terminal measurements can be avoided, including the impact of the series resistance of the ITO outside the active area or the fact that thermal runaway occurs which eventually destroys the device. However, with additional sensing contacts, it might become possible to detect the voltage decrease inside the device, since it is a typical feature of 4-wire measurements that the series resistance is excluded.

Experimental Standardized samples are used which are produced for tracking purposes to continuously check processing quality. OLEDs for 4-wire crossbar measurements are fabricated by thermal vapor deposition in high vacuum. After cleaning of the prestructured ITO-glass substrates, a p-doped/intrinsic/n-doped layer configuration is realized, using 30 nm MeO-TPD:F6TCNNQ (2wt%), 10 nm NPB, a ca. 20 nm thick emitter system, 10 nm BAlq2, 30 nm BPhen:Cs (ratio: 1:1). 100 nm Al is used as the top electrode. For the emitter system, 20 nm MADN:TBPe (1.5wt%) (blue), 6 nm TCTA:Ir(ppy)3 (8wt%) and 12 nm TPBI:Ir(ppy)3 (8wt%) (green), 20 nm NPB:Ir(MDQ)$_2$(acac) (10wt%) (red) are used. The glass substrate has a size of 2.54 cm in square and a thickness of 1.1 mm. The active area is approximately (2.54 mm)^2. 4-wire crossbar measurements are carried out with two source-measuring units (Keithley 2400) controlled by a home-built software. Similar OLED configurations have been published in Refs. [559, 560].

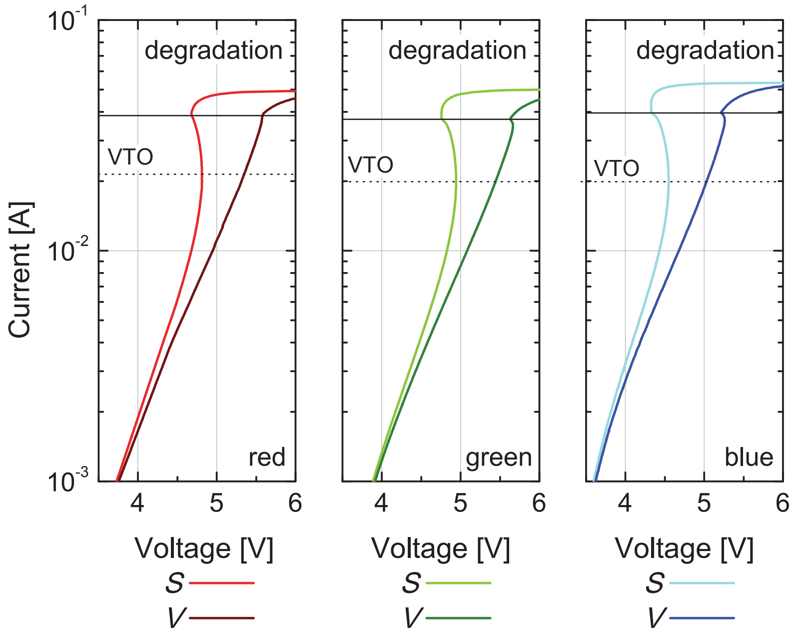

Figure 9.8: IV characteristics of the 4-wire crossbar measurement for a red, green, and blue OLED. The total current is plotted over the voltage V, to drive the current and the measured voltage S at the sensing contact. Starting with 20 mA voltages are decreasing with increasing current, indicating the NDR effect. A dotted line denotes this voltage turnover (VTO). This happens before samples degrade (black solid line) due to overheat in the range between 35 mA and 40 mA.

4-wire crossbar measurement To realize a 4-wire crossbar measurement, the encapsulation glass is removed in a glovebox. After this procedure, the current-voltage characteristics of the OLEDs remain unchanged. All contacts are enhanced with silver liquid to ensure proper connection to the contact needles. A picture of a sample after measurement can be seen in Fig. 9.7e). The measurements performed during operation of a red, green, and blue OLED are shown in Fig. 9.7a-c).

The results are plotted in Fig. 9.8 for a current sweep from 1 mA until degradation appears, with 500 measurement steps per decade. First, the current plotted over the applied voltage V is discussed. The corresponding data coincide with a normal 2-wire measurement. With rising voltages the current also rises until ca. 40 mA, which will unavoidably lead to the degradation of the sample due to self-heating. Since these OLED layer structures become highly ohmic while degrading, the applied voltage V rises strongly in the constant current mode. Thus, the dissipated power increases and heats up the device, accelerating the degradation behind the kink in the IV curves. Besides this, a 2-wire measurement of an OLED will not disclose any special effects.

Now, the currents plotted over the sensed voltage S is focused. In contrast to the previous measurement, a qualitatively different result is obtained. Beginning from 1 mA, both types of curves deviate from each other, indicating the beginning of self-heating. Thermal imaging of an encapsulated sample confirms this result [494]. Most interestingly, when reaching about 20 mA, the sense contacts show a voltage turnover, clearly distinguishable from the onset of the degradation. As a result, the 4-wire crossbar measurement proves the presence of NDR due to self-heating in a red, a green, and a blue OLED.

Electrothermal OLED simulations The voltage V and the voltage S differ under self-heating, thus it is expected that the voltage drop across the device is not uniform anymore, leading to inhomogeneous current transport and heat dissipation. With the help of an electrothermal network simulation made by the freely available program LTSpice IV (Linear Technology) and a self-made circuit generator script, the processes taking place in the OLED are investigated. In Ref. [437], a product ansatz of an isothermal power law current-voltage characteristic and an Arrhenius-like conductivity-temperature law has been successfully used to explain S-NDR phenomena in n-doped/intrinsic/n-doped C_{60} devices given by

$$I(V,T) = I_{\mathrm{ref}} \left(\frac{V}{V_{\mathrm{ref}}} \right)^{\alpha} \exp \left[-\frac{E_{\mathrm{act}}}{k_{\mathrm{B}}} \left(\frac{1}{T} - \frac{1}{T_{\mathrm{a}}} \right) \right] , \tag{9.2}$$

where α is the exponent of the power law, T is the device temperature, E_{act} is the activation energy of the conductivity, and T_{a} is the ambient temperature. I_{ref} and V_{ref} are reference values for current and voltage determined from an isothermal IV curve. The implementation of this thermistor model for the multi-physics network simulation is based on Ref. [561]. An array of $(m = 10) \times (n = 10)$ thermistor devices now represents the active area and the current of each thermistor I_{ij} equals the charge flow through the OLED layer stack for a certain part of the active area. For simplicity, it is assumed that the metal electrode (cathode) of the OLED has such a low sheet resistance in comparison to the ITO (anode) that its influence can be neglected. Thus, all upper connections of the thermistor array are directly connected to each other. The anode is modeled by connecting all lower electrical contacts of the thermistor array via a network of resistors corresponding to a sheet resistance of $26.5\,\Omega$. Furthermore, the thermistor array is coupled to a thermal network, modeling both the glass substrate and the heat transport into the environment. In this thermal network, a resistor corresponds to a thermal resistance, a voltage represents a temperature difference, and a current represents a heat flow. The thermal network is a 3D resistor network and includes regions outside the electrically active area. Besides heat generated by the thermistor devices, the simulation incorporates voltage drops along the anode, producing a further heat source fed into thermal network. Details about the multi-physics network model can be found in Ref. [494]. For a comparison of experiment and simulation, further 4-wire crossbar measurements are performed on a green OLED, mounted onto a copper block. The results are shown in Fig. 9.9. The power law describing the isothermal current-voltage characteristic of the OLED is easily fitted by defining a reference point where no self-heating occurs. Here, this is $I_{\mathrm{ref}} = 1\,\mathrm{mA}$ and $V_{\mathrm{ref}} = 3.942\,\mathrm{V}$ so that the IV curve of the total thermistor array is fixed to this point and the correct increase can be tuned by adjusting the exponent of the power law to $\alpha = 8.7$. The fact that a part of the applied power is coupled out as light is considered by reducing the generated heat by 20%. For simplicity, this value is kept constant.

The thermal system of the OLED can be described by a heat flow downwards into the glass substrate and upwards into the nitrogen atmosphere. A lateral flow to the substrate given by the thin electrodes or the organic molecular layers is neglected (c. Ref. [318]). The use of a simplified resistor network to model the heat transfer requires a well-defined and easy to describe thermal system. Therefore, the glass substrate is fixed to a copper block via heat sink paste to ensure proper thermal contact. The heat transfer from the OLED into the glass substrate and from the glass substrate into the copper block is supposed as ideal. Since the large copper block has a high heat conductivity (400 W/m/K), its temperature can be assumed to correspond to the

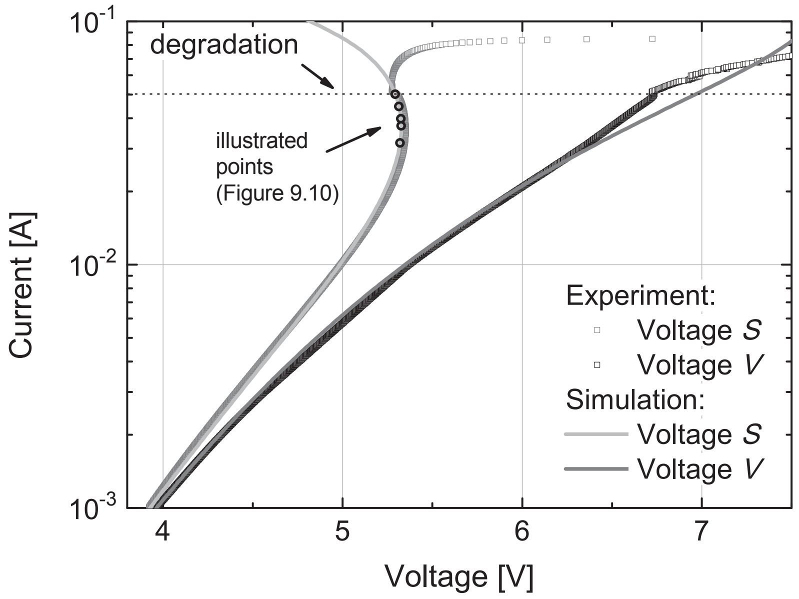

Figure 9.9: Simulated and measured IV characteristics of the 4-wire crossbar experiment, using the green OLED. The simulation of the sensing voltage *S* reproduces the experiment up to the point where the device starts to degrade. Small black circles indicate the currents at which simulated current density and temperature are presented in Fig. 9.10.

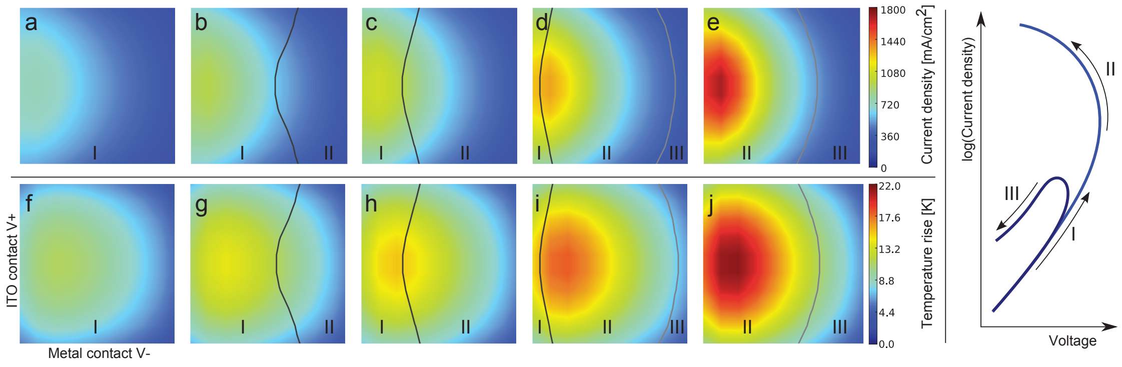

Figure 9.10: Simulated distributions of current density a)-e) and temperature rise f) - j) for total currents of 31.6 mA, 37.2 mA, 39.8 mA, 44.7 mA and 50.1 mA as marked in Fig 9.9. The schematic diagram shows the three operation regimes in a current-voltage plot of a thermistor. Normal (I): Increasing current density and voltage. S-NDR (II): Increasing current density while voltage decreases. Switched-back (III): Both, current density and voltage decreases. The schematic IV curve visualizes the different operation modes for each thermistor.

ambient temperature T_a. Thus, the limiting factor for heat transport is the thermal conductivity of glass, chosen to be 1.8 W/m/K. In the simulation, a variation of this parameter shifts the point of the voltage turnover to higher or lower currents along the normally measured curve. For the heat flow upwards from the OLED to air, a rather overestimated heat transfer coefficient of 10 W/m^2/K is used, anyhow still realizing a minor heat flow with respect to that realized by the glass substrate and the copper block.

Besides modeling the thermal environment, the most important parameter of the system is the activation energy E_{act} of the OLED, used in Eq. (9.2). This parameter influences the shape of the sensed current-voltage curve, leading to a stronger curvature with increasing activation energy. By using $E_{\mathrm{act}} = 25\,k_{\mathrm{B}}T_0$, a good agreement between experiment and simulation is achieved (cf. Ref. [494]). Although this model of thermistors, electrical resistors, and thermal resistors is simple, it accounts for all qualitative aspects of the system described above. Furthermore, it allows to reproduce the experimental results, as visualized in Fig. 9.9. Degradation effects above 50 mA are not incorporated and no agreement can be achieved above this value.

A closer look into the simulated distribution of currents and temperature is given in Fig. 9.10 for five different values of the total device currents as shown in Fig. 9.9. The simulation results are interpolated and visualized with matplotlib (contourf-function, linear interpolation), which does not change the value range or the local occurrence of NDR regions. Each picture shows the active area of the OLED sample. The electrodes are connected as shown in Fig. 9.7d), meaning that the current essentially flows from the left side (ITO) through the OLED stack and leaves at the bottom side via the metal electrode. With increase of the total current, the current density in the device will strongly rise in the left region of the active area while at the opposite side the current seems to change less. A similar behavior can be seen for the temperature increase which appears more widened but still is mainly located close to the left edge of the active area. Current density and temperature rise tend to consolidate more and more towards the left region whereas close to the right edge, they remain nearly unaffected by changes of the total applied current or voltage.

From the fact that declining voltages have been obtained in Fig. 9.8, it is essential to investigate the local current I_{ij} and the local voltage V_{ij} in terms of NDR. Therefore, local differential resistance

$$R_{\mathrm{diff,ij}} = \frac{dV_{\mathrm{ij}}}{dI_{\mathrm{ij}}} \tag{9.3}$$

is defined as the differential of the local voltages and currents across the OLED layers between top and bottom contact. The contour $R_{\mathrm{diff,ij}} = 0$ is indicated by a dark gray line in Fig. 9.10, separating region I and region II. Region I behaves normally, showing increasing currents while the voltages are rising. In contrast, region II has a local NDR, and thus currents are rising under decreasing voltages. It is obvious that regions of NDR are expanding backwards from the right to the left with the increase of the total device current. They appear first with the occurrence of the voltage turnover of the sensed voltage S in the 4-wire crossbar measurement.

However, by reaching a certain current level, a new region III enters into the device from the right. Surprisingly, this region has once more a positive differential resistance, similar to the normally behaving region I. To understand this phenomenon, the differential resistance has to be analyzed in more detail. In Fig. 9.11, a table of four possible configurations is shown. The local

voltage current	$\frac{dV_{\mathrm{ij}}}{dV} > 0$	$\frac{dV_{\mathrm{ij}}}{dV} < 0$
$\frac{dI_{\mathrm{ij}}}{dI} > 0$	$\frac{dV_{\mathrm{ij}}}{dI_{\mathrm{ij}}} > 0$ normal (I)	$\frac{dV_{\mathrm{ij}}}{dI_{\mathrm{ij}}} < 0$ S-NDR (II)
$\frac{dI_{\mathrm{ij}}}{dI} < 0$	$\frac{dV_{\mathrm{ij}}}{dI_{\mathrm{ij}}} < 0$ N-NDR (not present)	$\frac{dV_{\mathrm{ij}}}{dI_{\mathrm{ij}}} > 0$ switched-back (III)

Figure 9.11: The table visualizes the four different types of differential resistance. In a thermistor array, three of them are possible: normal (I), S-NDR (II), and switched-back (III).

change in voltage is characterized by dV_{ij}/dV, and analogously for currents, dI_{ij}/dI characterizes the local change in current. In a normal operation mode, currents and voltages increase together with their external counterparts, while in an S-shaped NDR (S-NDR) region, currents will increase for decreasing externally applied voltages V. A very interesting configuration is realized when local currents and voltages decline at the same time, even though externally applied currents and voltages increase further. By comparison of the individual terms within the simulation result, it is found that in region III the OLED indeed shows such a strange behavior. It can be fully understood considering the decreasing local voltages in region II. Due to the fact that the ITO electrode is contacted from the left side, OLED regions at the opposite side might not generate enough power dissipation to heat up and reach a local NDR. Then they are supplied with the reduced voltage after the lateral passage of the NDR region (II). Since this region has declining voltages, in region III the OLED layer stack does only "notice" a declining voltage and consequently the current density is switched back. To give a simpler picture of that mechanism, calculations of three parallel thermistors coupled by series resistors are provided in the Appendix Sec. A.6. There it is shown that in a one-dimensional thermistor chain, all thermistors behind the first one are instantly switched back if no thermal coupling exists between them. If thermal coupling is incorporated, due to the heat exchange between individual thermistors, the abrupt switch back is replaced by a smoother transition similar to the simulations of the two-dimensional thermistor array presented in Fig. 9.10.

The fourth configuration in Fig. 9.11 is a decrease of the current accompanied by increasing voltages. This operation mode would correspond to an N-shaped NDR and is not present in this system due to the nature of the self-heating phenomena. The operation of region I, II, and III is further visualized in the schematic IV curve of Fig. 9.10. Please note, however, that due to the thermal coupling, every thermistor in the network has its own dependence $I(V, T)$ on voltage and temperature.

9.5 INTERMEDIATE SUMMARY

In this chapter, the interplay between temperature activated conductivity and self-heating has been discussed. The motivation for these investigations are the fact that transmission currents in C_{60} triodes are stimulated by temperature, showing activation energies clearly above $4\,k_B T_0$. Analog to NTC thermistors, this value is high enough to lead to such a strong electrothermal feedback that operation with NDR occurs. This has been demonstrated by thermal switching in nin-C_{60} crossbar devices and an excellent fit with a purely thermal theory is achieved, using parameters which have been obtained by independent experiments. Since it is common for organic semiconductors to have a temperature activated conductivity, the results can be transferred to the whole material class. Especially for C_{60} triodes as investigated in this thesis, self-heating is a major problem which could lead to thermal runaway and subsequently thermal breakdown. Indeed, this could explain why particular C_{60} triodes with a small active area and a low limitation by a series resistance are rapidly destroyed if the voltage reaches 3 V to 4 V, as observed in experiment. However, for a more detailed description of NDR effects due to self-heating in vertical organic triodes, further investigations and an improved setup are required which will be able to measure decreasing driving voltages under rising transmission currents. For a two-terminal crossbar device, a simple measurement setup called '4-wire crossbar' is proposed and tested on OLEDs. NDR due to self-heating has been clearly demonstrated before the degradation of the samples started. To understand the essential processes in such a laterally expanded device, a SPICE simulation with a two-dimensional thermistor array has been performed. The result shows that different parts of the device operate in different modes. Besides the normal operation mode, the device can show regions with local NDR after the turnover voltage is surpassed. Most interestingly, with a further increase in the total current flow, a new kind of operation mode enters as a region where currents and voltages are switched back. From that point on, the inhomogeneity of current flow will drastically increase. Thus, the described effect has a huge impact on brightness inhomogeneities in OLED lighting applications, but also on the understanding of current flow in vertical organic devices in general.

10 CONCLUSION AND OUTLOOK

10.1 CONCLUSION

A vertical organic transistor with a permeable base electrode using the semiconductor C_{60} is introduced. Benefiting from the high charge carrier mobility of C_{60}, extraordinarily high current densities and switching speeds are reached. In combination with the strongly reduced transfer length for charge carriers in the vertical triode, the device is a potential candidate for high performance applications. Indeed, the parameters achieved are already promising: Outstandingly high current densities of 10 A/cm^2 are realized at a low driving voltage in the range of a few Volts. Even at 0.5 V, the transistor can be operated. Although the on/off ratio is already in the range of 3 to 4 orders of magnitude and switching of the current can clearly be demonstrated, a larger on/off ratio in the range of 10^5 to 10^6 is desirable for future applications in order to reduce power consumption in the off-state, reduce crosstalk effects in an array configuration, or realize high contrast values in OLED based displays. A small subthreshold slope of ca. 200 mV/decade enables switching between the off-state and the on-state in a narrow range of the base-emitter voltage, so that in logic circuits, e.g. an inverter circuit, a high voltage gain can be expected, accompanied by a low power consumption. The vertical organic triodes further reach a pronounced current gain of up to 600 and, even in the on-state, a current gain of 100 is preserved, enough for applications that are usually realized with conventional bipolar junction transistors. Samples with a larger active area reach a transconductance of 30 mS (750 S/cm^2), and samples with a small active area achieve up to 5 mS (12500 mS/cm^2). Therefore, the best results exceed those of an OFET fabricated with a similar low resolution shadow mask ($L = 10\,\mu$m) (s. Sec. 3.1.4) by more than one order of magnitude. Because of the high transconductance of the devices, small signals can be processed at very high frequencies and a high switching speed is achieved. Rise times of 380 ns can be measured in pulsed mode and correspond to transit frequencies of ca. 1 MHz, further confirmed by the gain-bandwidth product of an inverter circuit using a vertical C_{60} triode.

In order to reach this performance, various treatments and techniques have been applied. Air exposure of the base electrode proves to be essential for device function. Electrically passivating the electrode surface by a ca. 2 nm thin native Al oxide and the annealing of the devices after fabrication changes the morphology of the base electrode. As a consequence, openings are formed in the central electrode, enabling charge transfer between the upper and the lower semiconductor layer. Only by combining both methods, working devices with high charge carrier transmission and current gain are realized. Based on this result, a further optimization was performed. It turns out that the alignment of the electrode is crucial for high performance operation. Even if the grid electrode enables superior charge carrier transmission, a slight misalignment of the masks can drastically reduce the measured current gain. An exclusive overlap of emitter and base reduces the device performance because it leads to increasing base currents due to the non-negligible leakage current through the surface oxide of the base electrode. As a solution, indirect structuring is introduced. Insulating layers are inserted between the emitter and the base electrode, defining a structured active area in which all electrodes overlap. This method does not only prevent leakage currents in misaligned areas, but it becomes a prerequisite for downscaling the device area and later integration in larger circuits. For example, active areas down to 200 µm times 200 µm are realized, helping to reduce the influence of external series resistances, and shifting the start of the self-heating regime to higher power densities. Thus, extraordinarily high current densities are measured. Another important optimization consists in the use of molecular doping. The insertion of a doped layer next to the emitter realizes an Ohmic contact at the interface, so that the transmitted current is greatly enhanced with respect to a non-doped sample. As a consequence, contact resistance plays no role, in sharp contrast to conventional OFETs. Further, contact doping also increases the current gain as a result of the electrical feedback present in the device. Variations of the semiconductor layer thickness indicate that the transport through the intrinsic layer hampers the charge flow. Consequently, a reduction of emitter layer thickness to 50 nm yields the best performance. Thus, the "sandwich"-architecture of the vertical organic triode is ideal to insert further functional optimization layers with a minimum effort. Especially if these layers are inserted in the base-emitter diode, the morphology of the grid electrode will not be disturbed, depending instead on the growth of the layers in the base-collector diode. Therefore, optimization of the grid, the charge transport, as well as structuring the active area can be done without influencing each other.

All these optimization steps are driven by an improved understanding of vertical organic triodes. Most importantly, the results point to an operation mechanism related to a permeable base electrode perforated by nano-size pinholes. As a consequence, a direct connection by semiconducting material exists between the upper and the lower C_{60} layer, enabling charges to be transmitted through the base electrode. This finding is supported from a structural analysis by TEM and XPS measurements, revealing regions of the base electrode where Al is not present, which can be interpreted as pinholes forming and enlarging by annealing the sample after fabrication. Electronically, the bidirectional operation allowing either to use the top or the bottom electrode as the emitter, as well as a characteristic electric feedback in the devices further allows to understand a vertical organic triode as a permeable base transistor with a nano-porous electrode. However, the STEM measurements reveal that such openings in the base electrode typically have a diameter below 5 nm and rather large distances between them, occupying less than 1 % of the area. In order to reach a high charge carrier transmission, a passivation of the base electrode is proven to be mandatory. This is achieved by the air exposure of the base electrode, forming a thin native oxide on the full surface (both sides) of the Al electrode. The oxide layer does not only reduce the leakage current into the base, but it also leads to a charge accumulation region in front of it, as known from MOS diodes. Therefore, on the emitter side, a highly conductive two-dimensional layer of accumulated charges evolves which is beneficial for charge transport from impermeable regions of the base electrode to an opening where charge carrier transmission can happen. Thus, the passivation of the base electrode is more than an electrical insulator: It introduces a device operation similar to an organic field-effect transistor, namely switching the conductivity of the charge channel zone. Besides being a nano-porous permeable base transistor, a vertical organic triode also forms an organic field-effect transistor based upon a special non-lateral geometry. As a consequence, base currents are not needed in order to drive the transistor in contrast to a bipolar junction transistor. In principle, the vertical organic triode could have characteristics similar to an OFET, e.g. a huge current gain, but with a much better on-state performance due to the strongly reduced device dimensions in vertical direction.

High power densities accompany the high current densities, leading to substantial self-heating in the devices. Due to the temperature activation of their conductivity, organic semiconductors essentially act as thermistor devices, showing an S-NDR related bistability and thermal switching. This phenomenon introduces an instability of the device via thermal runaway. Moreover, the current flow can become inhomogeneous, as demonstrated for a simple crossbar structure using 4-wire measurements. An exact knowledge about self-heating in organic semiconductor devices will help to realize high performance and stable vertical organic transistors operating at the maximum speed. A deeper understanding of self-heating will help to optimize the brightness homogeneity of OLED lighting panels at very high light output.

10.2 OUTLOOK

Based on this improved understanding, several studies can be thought of, continuing the progress in the field of vertical organic triodes, especially for those based on C_{60}. Now that it is obvious in which way the morphology of the base electrode plays a critical role for charge transmission, processing parameters can be varied in order to achieve an improved pinhole formation. For example, a different evaporation rate and substrate temperature used either for the base or the lower C_{60} layer are likely to change the growth of Al. This might also lead to an annealing-free pinhole formation resulting in improved device characteristics. However, the annealing is not only advantageous for changes of the base morphology, but can help to stabilize the device performance by removing trap states and by forestalling changes by self-heating. In the context of improved charge transmission, the leakage current through the thin surface oxide layer of the base electrode has to be minimized. If it will be possible to enhance the oxide thickness, higher current gain as well as higher switching speed due to the minimized capacitance are in reach. A resulting slightly higher gate-source voltage will not be a critical issue because the overall voltage range will remain quite low. Another opportunity to increase the current gain relies on an enhanced charge carrier mobility of the organic semiconductor. It is known that a surface treatment of the gate dielectric and adaption of the processing temperatures like substrate temperature can greatly enhance the field-effect mobility of C_{60} to values above $6\,\mathrm{cm^2/Vs}$. Thus, procedures like self-assembled monolayers on the base electrode have the potential to enhance the oxide quality and to improve the morphological formation of the upper C_{60} layer typically used as the emitter layer. Further improvements can be expected by tuning the doping concentration as well as the thickness of the intrinsic emitter and collector layer. In analogy to conventional bipolar junction transistors, highly doped and thin emitter regions together with sparsely doped thicker collector regions might be an alternative for vertical organic triodes, too. This would improve the breakdown voltage in the off-state, an often forgotten but important parameter. If the transistor is used as a switch or amplifier in series with a load, the driven power can be easily enhanced by increasing the voltage applied to the circuit. However, in the off-state, most of the voltage drops across the transistor, mainly between the base and collector. A thicker collector region would reduce the electric field and thus increase the breakdown voltage. Further, a realization of spatial doping profiles would be an opportunity to control the Fermi level alignment in the device and thereby the threshold voltage. Related to this are studies of the long-term device stability. Especially the threshold voltage is a critical parameter for circuit design because any shift over time can lead to malfunction, or in the worst case even to an excess voltage of following devices resulting in their destruction. Furthermore, Joule self-heating in organic semiconductor devices has to be studied in detail when highest current densities and switching speeds are required. On the one side, electrothermal feedback due to self-heating can reduce the driving voltage at high current densities compared to an isothermal device, so that the power consumption of the transistor shrinks and the charge carrier mobility increases. Both effects increase the transistor performance. However, extensive heating of the device potentially influences the device stability and eventually leads to the destruction of the device by thermal runaway. Hence, an exact knowledge of the positive feedback loop initiated by the dissipation of thermal power from the device into the environment represents a key factor to increase the performance as much as possible. Self-heating becomes even more relevant when flexible plastic substrates are used in future. They enable bending which is one of the main advantages of organic and plastic electronics in general. At the same time, they exhibit a one order of magnitude lower heat conduction than glass, and it is clear that these light weight flexible devices will not be equipped with a heavy rigid copper block in order to improve cooling. Thus, it can be expected that self-heating studies will become more decisive in the future if the performance reached in the lab has to be transferred into products. Finally, a point is reached where experiments have to be supplemented more and more by simulations. Based on the findings in this work, it has become possible to model the device by accounting for drift and diffusion currents in the precise geometry of the device. Then, present restrictions of the current flow can be resolved in more detail. It will be of great interest to analyze in which way geometrical aspects influence the overall device performance, including the size of the openings and their distribution, material aspects like the conductivity of the intrinsic layer, or the conductivity in the charge accumulation zone.

Further investigations relying on the present work have now revealed the full potential of vertical organic triodes employing C_{60} as the main material and doping as an efficient tool to eliminate contact resistances[1]. By improving the concept of indirect structuring using a more suitable insulating material and an adapted electrode layout, the performance achieved in this work has been further improved. At a driving voltage of 1 V, current densities of more than 10 A/cm^2 and a large transconductance are reached, allowing for a transit frequency of more than 2 MHz. Most interestingly, the on/off ratio has been greatly improved to values close to seven orders of magnitude, mainly by a substantial decrease of leakage currents. Thus, the exponential regime of the base

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[1] Mentioned data are from the master thesis of Markus Klinger, prepared in 2014 at the Institut für Angewandte Photophysik, TU Dresden with the title "Optimization of Vertical C_{60} Triodes for High Frequency Applications" (as yet unpublished).

sweep is now more pronounced, revealing a subthreshold slope of 100 mV/decade, close to the ideal value.

For a long time, vertical organic transistors have been proposed as candidates to overcome restrictions of lateral organic field-effect transistors. Despite the achievements reached in the field, the performance obtained was not yet able to compete with conventional technologies based on low-cost structuring methods. In this work, it has become obvious that fully vacuum deposited vertical organic transistors using low resolution and cheap shadow masks can outperform their counterparts with lateral current flow. The great improvement in current density, switching speed, and power consumption enables completely new fields of applications. However, typical characteristics of OFETs like a pronounced current saturation in the output characteristics are missing for vertical organic triodes, probably due to the onset of short channel effects. It is conceivable that OFETs and VOTs will address different applications. While the former are ideal for logic circuits and prototypical usage as switching or driving transistor for pixels in displays, the latter are more suited for analog circuits where either small signals at high frequencies have to be processed, or where elevated power must be handled. Further, interesting applications include a discrete switch, e.g. to drive complete rows and columns in a display, because the large current densities predestinate VOTs to provide sufficient current for a large number of pixels on a minimal area. Due to the fact that they exhibit a current gain and a characteristic similar to inorganic bipolar junction transistors, similar applications can be addressed. For comparison, a BJT operating at 10 mA achieves transit frequencies in the range of 200 MHz[2] whereas a VOT based on organic materials with much smaller charge carrier mobilities is only 100 times slower at a similar current, so that there is still room for improvement. As a consequence, applications where highest frequencies are not needed can already be realized by using vertical organic transistor technology. Therefore, the achievements of this work open up the way to reconsider the usage of organic transistors by greatly extending the parameter range which can now be accessed.

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[2] Data taken from the data sheet of an npn-BJT BC547.

A APPENDIX

A.1 APPENDIX 1: ACCURACY OF THE CURRENT GAIN

Under the occurrence of current in reverse direction of the BC diode, a determination of the current gain by I_C/I_B leads to uncertainties. However, if the ratio r between the transmitted current and the BC leakage current I_{EC}/I_{BC} is large, one can estimate within which accuracy η the calculated value agrees with the current gain realized by the actual transmission. The following expression

$$\frac{I_C}{I_B} \leq \frac{I_C - I_{BC}}{I_B + I_{BC}}(1+\eta) = \frac{I_{EC}}{I_{EB}}(1+\eta) \tag{A.1}$$

must be fulfilled. One can show that the equation can be transformed into

$$\frac{1 + I_{BC}/I_{EC}}{1 - I_{BC}/I_{EB}} \leq 1+\eta \tag{A.2}$$

by the help of Equations 3.17 and by using $I_{EB} = -I_E - I_{EC}$,

$$1 + \frac{I_{BC}}{I_{EC}} \leq \left(1 + \frac{I_{BC}}{I_E + I_{EC}}\right)(1+\eta) \tag{A.3}$$

originates. This equation further transforms to

$$1 + \frac{I_{BC}}{I_{EC}} \leq \left(1 + \frac{I_{BC}}{I_{EC}\left(I_E/I_{EC} + 1\right)}\right)(1+\eta) \tag{A.4}$$

where the expressions for the ideal transmission $\alpha = -I_{EC}/I_E$, and the current ratio $r = I_{EC}/I_{BC}$ can be substituted. Transposing the equation finally leads to the expression

$$r \geq \left(1 + \frac{1+\eta}{1/\alpha - 1}\right)\frac{1}{\eta} \tag{A.5}$$

which can be used to determine the quality of the estimated current gain under the presence of a base-to-collector leakage current I_{BC}.

A.2 APPENDIX 2: FIT OF XRR MEASUREMENTS

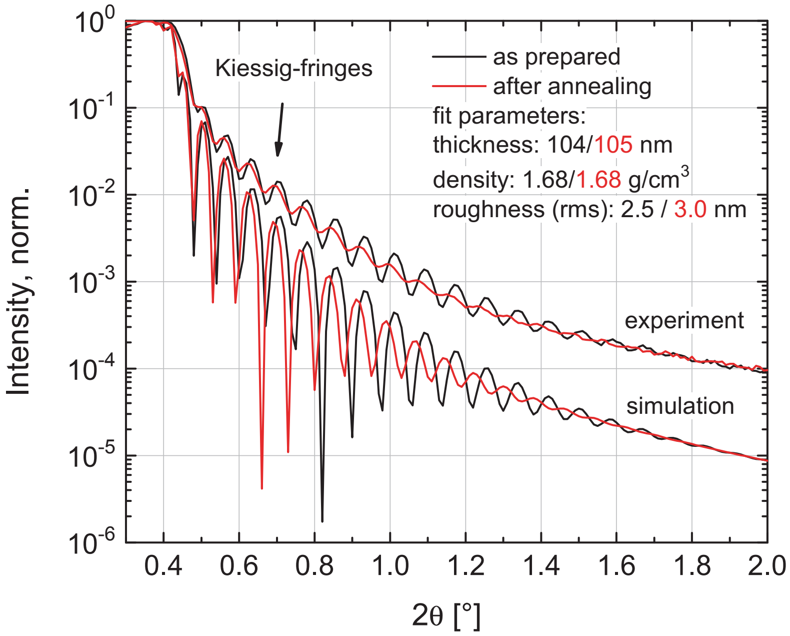

Figure A.1: Comparison between experiment and simulation of an XRR measurement of 100 nm C_{60} deposited on glass substrate before and after annealing for 2 h at 150 °C.

Figure A.1 shows an XRR measurement for 100 nm C_{60} deposited on a glass substrate before and after annealing for 2 h at 150 °C. Besides the experiment, simulated data using the program RefSim (Bruker AXS [562]) are presented to fit parameters like layer thickness, layer roughness, and material density.

The sample setup used for fitting consists of a glass substrate with a density of 2.2 g/cm^3 and a low roughness (rms) of 0.1 nm. These parameters are kept constant whereas the parameters of the C_{60} layer are varied to reach a qualitative accordance to the experiment. The density of C_{60} is set to 1.68 g/cm^3 and the layer thickness equals 104 nm, so that a similar periodicity of the Kiessig fringes is reproduced. After annealing, the density has not to be changed and the layer thickness slightly increases to 105 nm, matching again the periodicity of the pattern. Although the slope and the strength of the Kiessig fringes are not matched, the decay of the Kiessig fringes gives an information about the roughness of the layer. The fact that the oscillating signal vanishes at smaller angles after annealing can be reproduced in the simulation by increasing the C_{60} layer roughness (rms) from 2.5 nm to 3.0 nm. As the result, this measurement shows that the C_{60} layer is stable against annealing, but can undergo certain morphological changes at the surface which, however, do not drastically change the layer thickness or roughness.

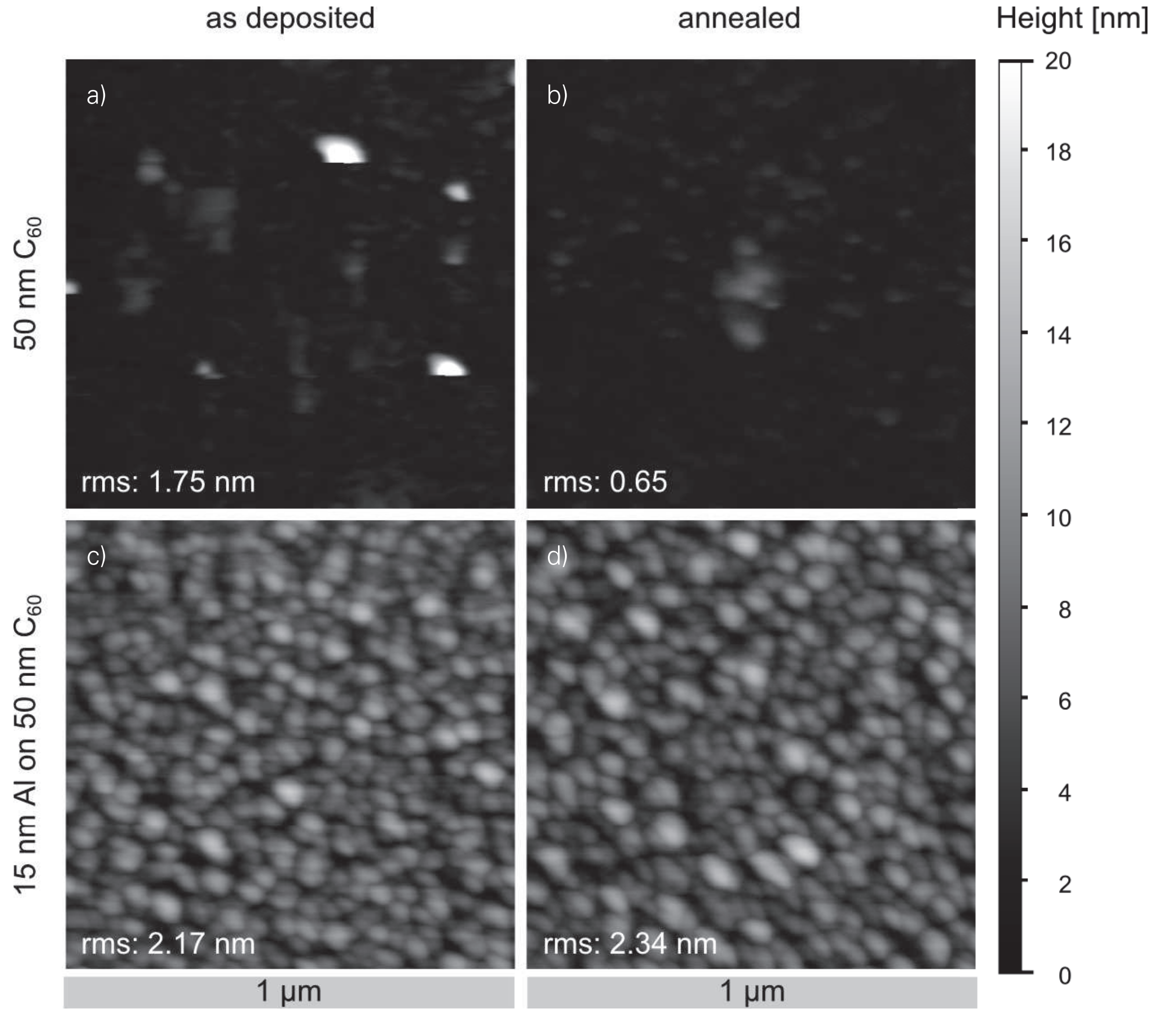

Figure A.2: AFM pictures of 50 nm C_{60} deposited on a glass substrate a) as prepared and b) annealed. Additional 15 nm Al can be seen in c) as prepared and d) annealed. Annealing is done at 150 °C for 2 h on a heat plate in a nitrogen atmosphere. The height scale is valid for all pictures. The surface of the pure C_{60} layer is quite flat but reveals some regions with a sudden increase in height with a lateral size of ca. 100 nm. The number of this regions seems to decrease after annealing or while measuring which hints to an adsorption of particles on the C_{60} surface, contributing mainly to the roughness. Furthermore, C_{60} covered by Al does not show similar features, independent from annealing, supporting that the C_{60} surface might attract some components from air. The annealing of the thin Al layer changes the roughness less.

A.3 APPENDIX 3: ATOMIC FORCE MICROSCOPY

Similar to the SEM measurements in Sec. 6.3, samples are fabricated for atomic force microscopy[1]. A 50 nm C_{60} film is deposited on a glass substrate. One half of the sample is further evaporated with additional 15 nm Al, representing the base electrode. Afterwards, a part of the sample is annealed at 150 °C, for 2 h on a hot plate in a nitrogen atmosphere. The result is shown in Fig. A.2 for all possible combination (with and without an Al top layer and before and after annealing). Images have been changed line by line to match similar height medians and for comparability, they have an equal height scale of 20 nm.

The C_{60} layer exhibits as prepared a very smooth surface ranging between a height 0 nm to 5 nm. However, there are particles on the surface in an irregular appearance, with a lateral dimension of around 100 nm and a vertical dimension above 20 nm. Moreover, the overall quality of the picture is low and it can be seen that some of the particles vanish during the measurement, leading to an abrupt missing of particles within the next scanned line. This points to an adsorption of compounds from the environment onto the surface. Even scanning on different position on the sample has not remedied this fact and the best measurement is already presented. After annealing, there are less particles but still remain on the surface, a further hint that they are not permanently stuck to the surface or are part of the surface. The roughness decreases from 1.74 nm to 0.65 nm during annealing, but it must be assumed that the particles increase the measured roughness of the surface. For example, in a region without a particle the roughness is below 0.5 nm, showing that C_{60} builds out very flat layers. Due to the quality of the measurement, an increase of roughness or a changed surface morphology as found by XRR measurements in Sec. 6.3 cannot be proven, but it is likely that drastic changes of the surface would have been visible if they occur. Likewise, the XRR measurements are performed in air and it should be mentioned that the corresponding results could be similarly affected by the adsorption of compounds from air. If these particles are part of the C_{60} layer itself, they should be also visible after the deposition of the Al layer, but in Fig. A.2c) and d), similar structures are not revealed. With the Al layer on top, the range of heights increases to around 20 nm, independently from the annealing, and the roughness changes only slightly from 2.17 nm to 2.34 nm by annealing. Since the C_{60} surface is quite smooth, the stronger variation of heights after deposition of Al points to the presence of thinner and thicker regions of Al. Thus, it might be possible to have regions thin enough to be not covered by Al and in that sense forming a pinhole. Nevertheless, the AFM measurement is found to be not an appropriate tool to prove the presence of the pinholes, because it cannot distinguish between different materials.

A.4 APPENDIX 4: TRANSMISSION ELECTRON MICROSCOPY

In order to verify that the STEM picture brightness is closely related to the 15 nm Al deposited on 50 nm C_{60}, Fig. A.3b) compares the brightness level with the X-ray intensity of the Al K_{α} radiation (using energy dispersive X-ray spectroscopy (EDX) upon line scanning as indicated in Fig. A.3.

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[1] Measurements are done with a Combiscope (AIST-NT)

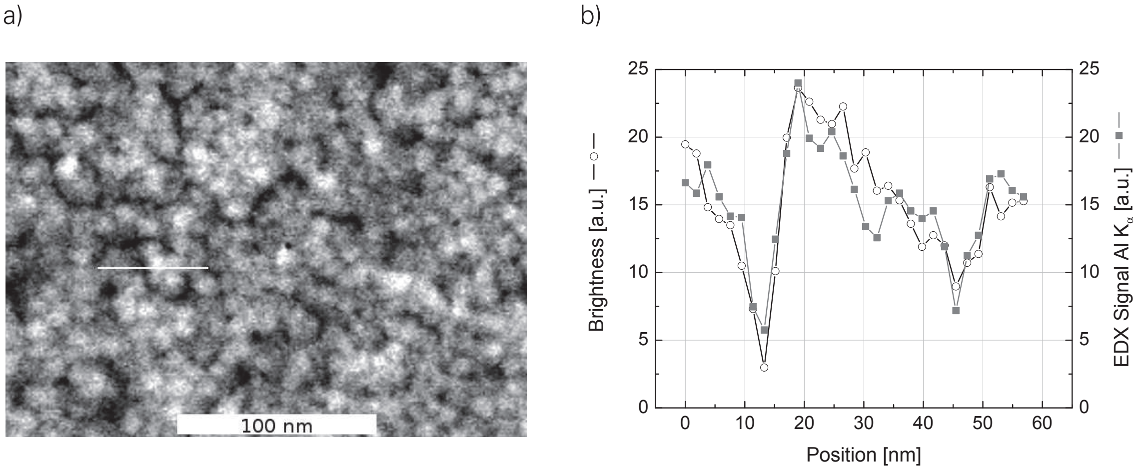

Figure A.3: STEM measurement of 15 nm Al on 50 nm C_{60}. a) A scan (white thin line) is performed in order to investigate the thickness variation in the Al layer. b) The brightness of the scan is compared to the intensity of the Al K_α radiation at each point. Each signal is normalized by the area under the curve and multiplied with 15 so that the median level agrees with deposited thickness of Al in nanometer. Both signals behave similar, revealing that STEM image brightness is strongly related to the Al layer thickness. The ratio between maximum and minimum values is in the range of 5. This strong thickness variation favors the formation of pinholes in the layer.

Under the assumption that the intensity is proportional to the layer thickness, both signals are normalized by the area underneath the curves because the overall intensity should then scale with the amount of deposited material. Moreover, the normalized curves are multiplied by a factor of 15 so that presented values correspond to the layer thickness measured in Nanometer. First, both signals show a strong correlation and thus one can assume that the STEM picture mainly shows the Al layer and the C_{60} layer underneath can be understood has a non-significant influence in comparison to the electron intensity scattered by the Al layer. Furthermore, values scale in a similar range using a comparable normalization so that the brightness of the STEM images shown in Sec. 6.3 can be used to deduce the layer thickness. Especially, each pixel with zero brightness has to be understood as a pinhole in the Al layer or a part of a larger one. Because Al atoms, interdiffusing into the C_{60} layer, contribute to the scattered intensity but do not necessarily have to disturb charge carrier transmission through a pinhole, even pixels with a brightness level slightly above zero could be part of a pinhole.

Conventional TEM (CTEM) is further used to investigate the Al grains and their modifications during the annealing step. Figure A.4 shows the result. The layer configuration equals the setup used in Sec. 6.3 with 15 nm Al deposited on 50 nm C_{60} and exposed to air afterwards. CTEM is done for samples as prepared and after annealing at 150 °C for 2 h. As substrate, a copper grid with a 20 nm thin carbon film is used. Images in Fig. A.4a) and b) are taken by slightly defocusing the sample to enlarge the contrast[2]. Thus, grain boundaries appear as bright lines, enabling a better distinction of individual Al grains. Before annealing, grain boundaries are visible but often not well pronounced and the transition from one grain to a neighboring grain is sometimes undefined. The size of the grains is in the range of 10 nm. After the annealing step, the grain boundaries have an increased visibility and single grains seems to differ more from their neighboring gains. Al grains seems to be slightly increased having a diameter in the range of 15 nm. This picture is in agreement with the STEM measurements shown in Sec. 6.3. Further, this is supported by CTEM

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[2] The focus is about 1 µm away from the Gaussian focus

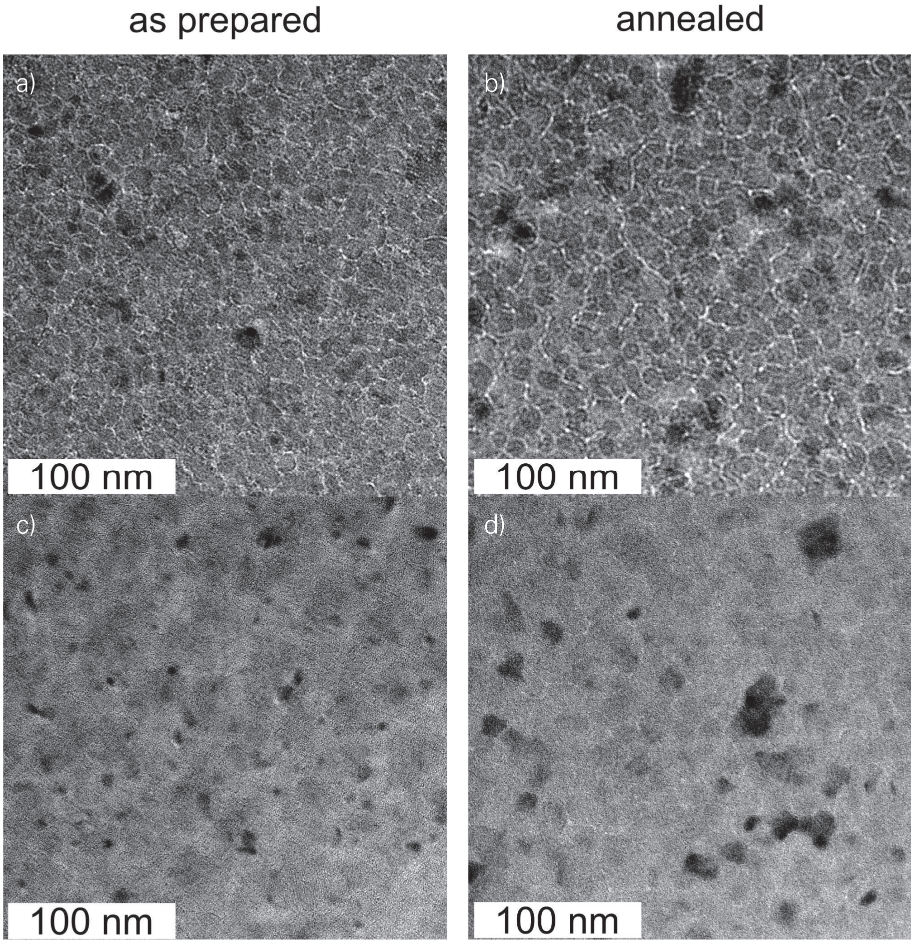

Figure A.4: Conventional TEM (CTEM) measurements of 15 nm Al deposited on 50 nm C_{60} as deposited (a) and c)) as well as after annealing (b) and d)). In the case of a) and b), the image is slightly defocused using a smaller aperture. Then, the picture gains additional contrast at cost of resolution. As a consequence, the grain boundaries of the Al layer are highlighted appearing brighter. In the case of c) and d), the image is taken in the focus but grain boundaries get less visible. All Al grains appear as a region of similar brightness.

measurement having no defocus as presented in Fig. A.4c) and d). Here, grain boundaries are hardly visible and particular grains appear as regions with homogeneous brightness. The variation of the brightness between different Al grains can be explained by electron channeling, describing the influence on the scattering process by different angles between lattice planes of the Al grains and the incident electron ray [563–565]. The grains where scattering is strongest can be seen best as they appear as dark regions in the bright field mode. For samples as prepared, these spots have a size between 5 to 10 nm whereas after annealing, there diameter increases by a factor of almost 2. As a consequence, it can be assumed that annealing leads to a reformation of the Al electrode. Smaller grains get incorporated in larger ones by adapting their orientation. As a consequence, single grains of the Al layer consolidate and thus generating space between them interpretable as a potential process for the formation of openings in the base electrode.

A.5 APPENDIX 5: DRIFT-DIFFUSION SIMULATION OF NIN DEVICES

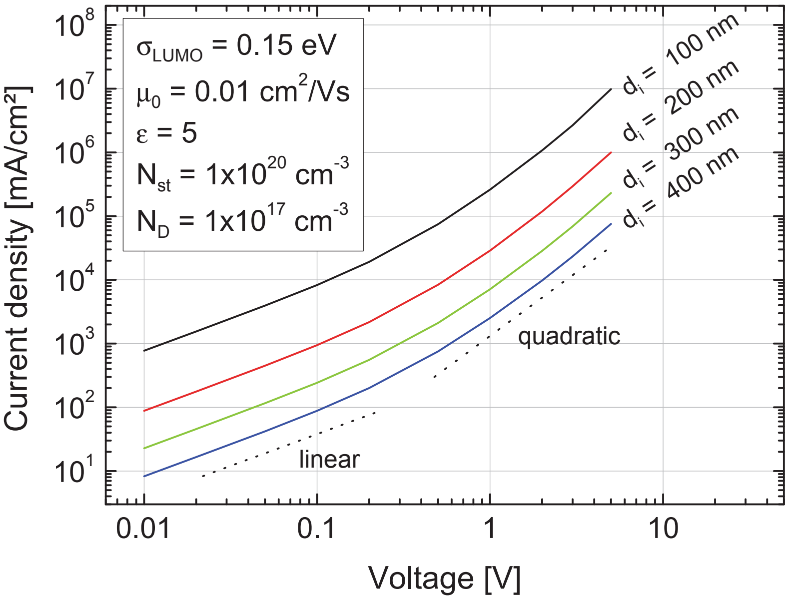

Figure A.5: Drift-diffusion simulation using the EGDM model of an nin device with 20 nm n-doped, intrinsic, and 20 nm n-doped layer. The thickness of the intrinsic layer ranges from 100 nm to 400 nm and the dependence on thickness is similar to the experiment shown in Sec. 9.2. After a linear regime, the currents increase quadratic or even slightly higher with voltage due to SCLC.

A drift-diffusion simulation is carried out for an nin device with the simulation program presented in Sec. 7.3, written by Matthias Schober and used in Ref. [106, 566]. The layer sequence consists of a 20 nm n-doped layer with a free charge carrier concentration of 1x10^{17} cm^{-3}, an intrinsic layer, and a second 20 nm thick doped layer. As valence (HOMO level) and conduction (LUMO level) band, values of C_{60} are taken. The mobility is described by the EGDM model as introduced in Sec. 2.1.4. Further parameters can be found in Fig. A.5, showing the thickness dependence from the intrinsic layer. Curves show a similar trend as observed in experiment (Sec. 9.2) and do

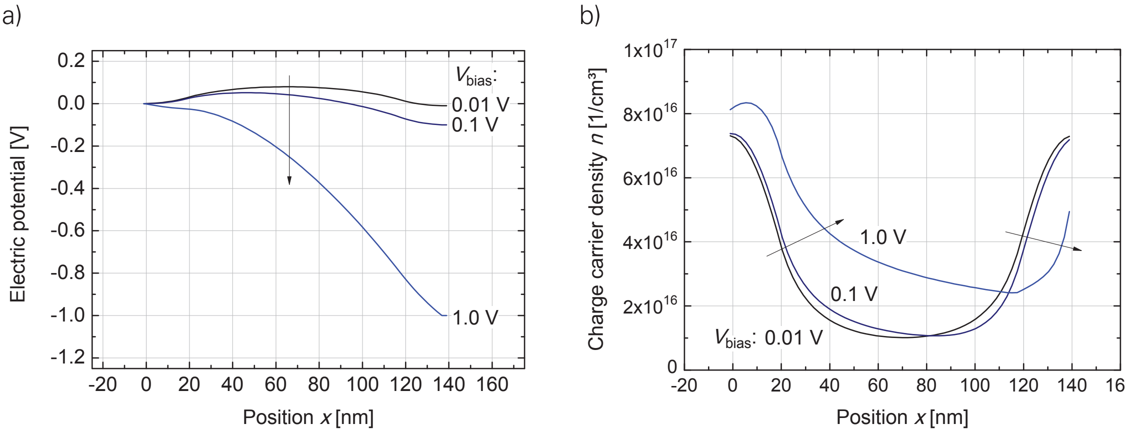

Figure A.6: Drift-diffusion simulation of an nin device. a) Electrical potential. For curves at voltages below 1 V, a diffusion component is required to overcome the potential maximum. b) Charge carrier density profiles. Even at very low voltages, charges are present in the center of the device. With increasing voltage, the charges merely concentrate close to the left charge injecting contact as predicted by SCLC.

also match similar current values at corresponding voltages. Please note that the nin-C_{60} crossbar device show a strong heating at the edges of the active area which is why a homogeneous current flow is not guaranteed so that a determination of parameters may be incorrect. However, from the qualitative accordance between experiment and simulation a basic analysis of the current transport through the device by the drift-diffusion simulation is justified.

Analog to the experiment, the curves show a linear law at voltages below 0.1 V. The currents are given by the conductivity of the sample due to its mobility and the charge carrier density already present at zero or very low voltages. As depicted in Fig. A.6a), there is a remaining amount of charge carriers in the intrinsic region at a voltage of 0.01 V although the simulation has been defined to have no charge carriers in this region. The reason is that electrons set free in the doped region diffuse into the intrinsic region, leading to charge carrier density of more than a tenth of the charge carrier density originally chosen in the doped layer. In this linear regime, the electrical potential has a maximum in the intrinsic region and thus the total current flow can be only realized if diffusion currents contribute there. However, due to the increasing charge carrier density towards the doped layer located at the ejecting contact (cf. Fig. A.6b)), drift current are also required to overcome the opposite directed diffusion currents. The situation changes if voltages of 1 V are reached and the current-voltage characteristic follows a quadratic law. This can be explained by space-charge limited currents, occurring when injected currents get limited by the mobility of the semiconductor. Now, the electrical potential in Fig. A.6a) is monotonically decreasing, leading to an overall contribution of drift currents in the device. Furthermore, the charge carrier density gets more and more asymmetric with a higher amount of charges near the injecting contact, as predicted by the theory of SCLC (cf. Sec. 2.1.4). Please note that although quadratic laws are a feature of SCLC, they only occur if a constant charge carrier mobility is assumed. A charge carrier density or an electric field dependence of the charge carrier mobility realizes an increase of this parameter with rising voltage. As a consequence, current-voltage characteristics with power laws stronger than quadratic are expected.

In this simulation, no contribution from self-heating is accounted and thus no change in the conductivity is realized by higher power dissipation. Thus, no shoot up of the current density at voltages above 1 V due to thermal runaway occurs in comparison to the experimental data (cf. Sec. 9.2).

A.6 APPENDIX 6: A SIMPLE PARALLEL THERMISTOR CIRCUIT

Here, a simple thermistor circuit is presented which consists of three thermistors in parallel, helping to explain the propagation of the different operation regimes through the OLED device as shown in 9.4[3].

The network model is solved by the freely available software LTSpice IV (Linear Technology). It is a simulation program with integrated circuit emphasis (SPICE). For modeling, the thermistor device is defined as published by Keskin [561] with the further implementation of a power law for the isothermal current-voltage characteristic of the thermistor. The power law is defined by a reference point (I_{ref}, V_{ref} which must be a point on the isothermal IV curve, and an exponent α. The thermistor model consists of two parts: An electrical part which defines the current-voltage characteristic with an Arrhenius-like temperature dependence of the conductivity, and a thermal part which accounts for a thermal heat flow where the electrical power dissipation acts as the heat source. In this thermal part, the potential difference necessary to conduct the heat flow into an externally connected thermal network corresponds to a temperature. Both parts of the thermistor model are in a feedback loop. The electrical part defines a dissipation power which is in turn used as a heat source by the thermal part to create a temperature. The resulting temperature increases the electrical conductivity within the electrical part.

To verify the thermistor model, a series connection of a thermistor and a resistor is simulated. For this simple circuit, an analytical solution can be derived [437]. In Fig. A.7, the SPICE model exactly reproduces the analytical solution for corresponding values of the resistor in series. Thus, the SPICE simulation is able to automatically reproduce the correct "S"-shaped self-consistent current-voltage characteristic under self-heating. Now, it is possible to extend the circuit to three parallel thermistors with series resistive coupling as shown in Fig. A.8. This configuration is the most simple one-dimensional analog to the simulation of the 4-wire crossbar presented in the publication. Simulation results are shown in Fig. A.9 for the following parameters: The reference point of the power law like isothermal current-voltage characteristic is set to $I_{\mathrm{ref}} = 1\,\mathrm{mA}$ and $V_{\mathrm{ref}} = 3.9\,\mathrm{V}$ with the current equally distributed to all three thermistor devices. The exponent of the power law is 8. The series resistor has a resistance of $R_{\mathrm{S}} = 100\,\Omega$ and the resistors, representing the sheet resistance, have a resistance of $R_{\mathrm{sh}} = 100\,\Omega$. The thermal resistance for each thermistor is chosen to be $R_{\mathrm{th}} = 1000\,\mathrm{K/W}$. If no thermal coupling is assumed (R_{coup} is infinity), all thermistor show a voltage return (cf. Fig. A.9c)), but only the first thermistor T1 in the chain has increasing currents over the whole range of applied voltages (cf. Fig. A.9a)). In this case, most of the current flows through the thermistor T1 next to the voltage supply. In Fig. A.9e), the respective current-voltage characteristics for each of the thermistors is shown. While the first thermistor shows the typical S-NDR behavior, the remaining thermistors reach a

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[3] The work presented in this section is submitted to Advanced Functional Materials

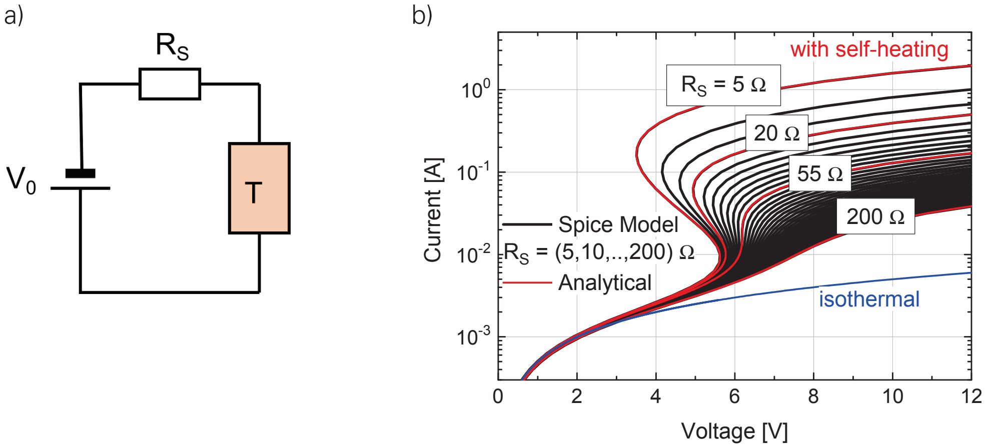

Figure A.7: a) Circuit of a thermistor and a resistor in series. b) The SPICE model of the thermistor perfectly matches the analytical solution for corresponding resistor values. The blue line represents the current-voltage characteristic of an isothermal thermistor or a thermistor with no activation energy. For the analytical solution, please compare Ref. [437].

maximum current and then return back on their IV curves because they are switched back by the decreasing voltage drop over the first thermistor which is passed to the next thermistors via the connecting resistors.

The situation changes if a thermal coupling of $R_{\text{coup}} = 1000\,\text{K/W}$ is integrated into the electrothermal circuit. Now, the first thermistor will still have the highest currents, but due to the heat exchange between the thermistor devices, the thermistors T2 and T3 can be heated up by the strong power dissipation of the first thermistor T1 and thus reach a higher conductivity. In that configuration, thermistors T2 and T3 can have increasing currents although the voltage drop is decreasing. Even though the voltage drop over T2 is reduced by T1, the higher temperature at T2 produced by the power dissipation of T1 can still result in increasing currents across T2. In Fig. A.9b), thermistor T2 has now increasing currents over the whole range of externally applied voltages. A further feature is that every thermistor reaches its maximum voltage drop at different externally applied voltages as visualized in Fig. A.9d). Finally, it can be seen that the thermal coupling of the thermistors changes the current-voltage characteristic of each thermistor completely (cf. Fig. A.9f)). If the thermistor T3 switches back, it does not return along the same IV curve. This can be explained by the fact that due to heating by neighboring thermistor devices, the individual thermistors can have an increased temperature even if the device itself does not yet show substantial self-heating.

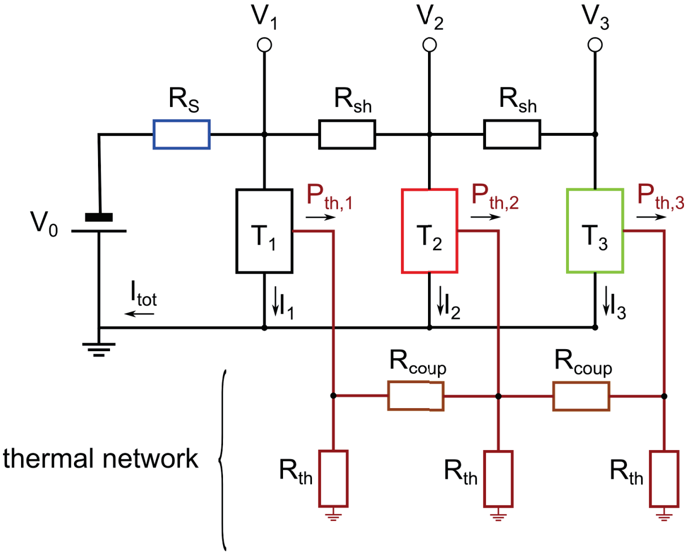

Figure A.8: Simplified SPICE circuit with three thermistors (T1, T2, T3) in parallel. They are electrically connected to each other by two resistors R_{sh}, representing the sheet resistance. The series resistor with the resistance R_{S} connects the circuit to the power supply with the applied voltage V_0. The voltages dropping over the thermistors are denoted by V_1, V_2, and V_3, respectively. Each thermistor is connected to a resistor R_{th}, representing the thermal resistance of each thermistor. Via the resistors R_{coup}, the thermistors can be coupled thermally.

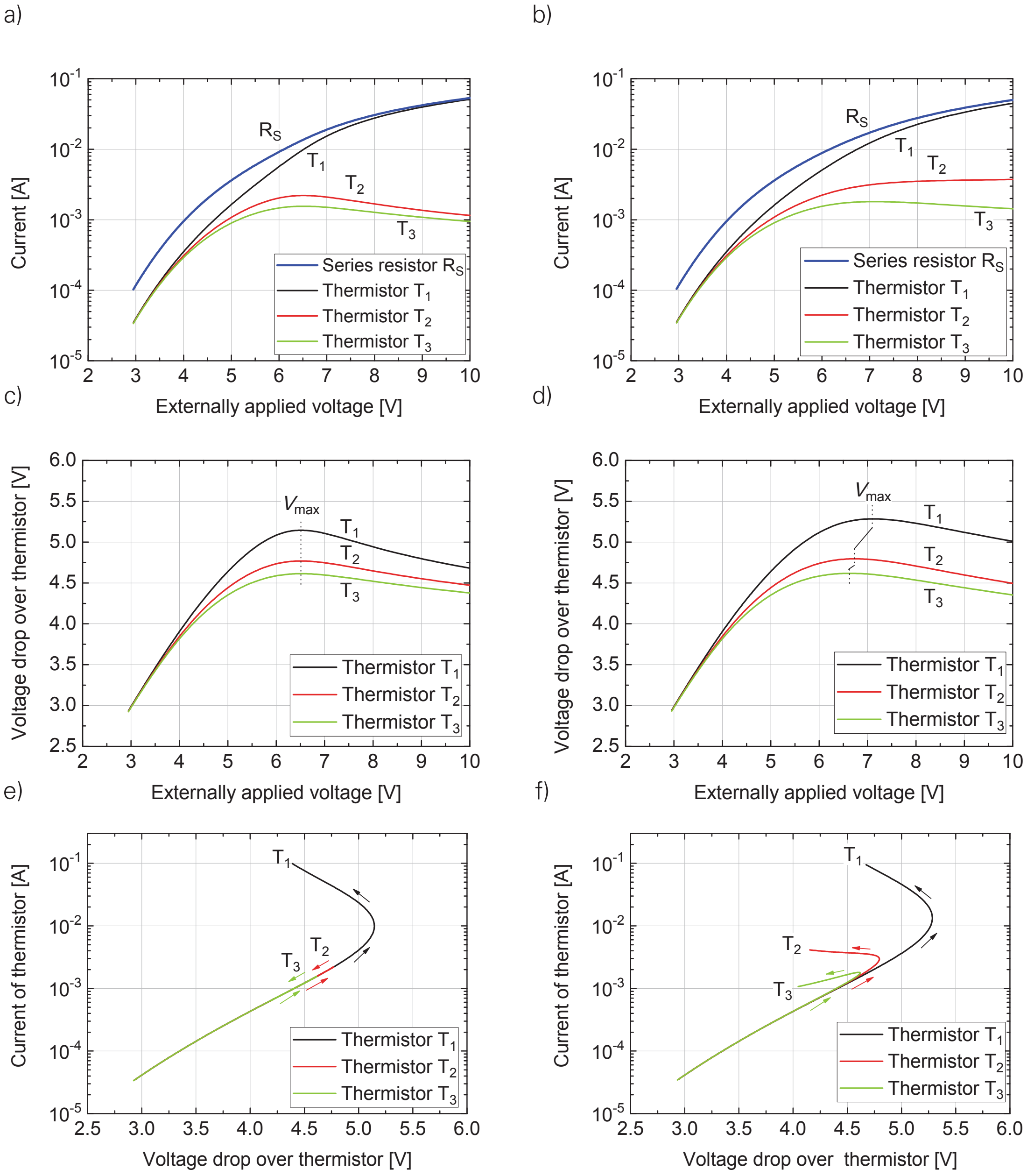

Figure A.9: Simulation results for the circuit presented in Fig. A.8. a), c) and e) Circuit without any thermal coupling between the thermistors ($R_{\text{coup}} = \infty$). b), d) and f) Thermal coupling with $R_{\text{coup}} = 1000\,\text{K/W}$.

LIST OF FIGURES

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ACKNOWLEDGMENT

The IAPP is a great place to conduct research: It has numerous fabrication and measurement setups as well as a pleasant atmosphere to meet people and create new ideas. Therefore, I am very grateful that Prof. Leo has supervised my PhD thesis and that he gave me the opportunity to work at the IAPP where I could also try out new ideas besides my original topic. I would like to acknowledge my second referee Prof. Dr. Henning Sirringhaus here, who has to work through this considerably extensive manuscript, too.

The possibility to work on vertical organic transistors is due to the engagement of Prof. Dr. Björn Lüssem who introduced these kind of devices at IAPP around 2009 and initiated the "Newdev" group. I really appreciate this decision, as the covered topic ranges from basic research to application relevant aspects, which I enjoyed a lot. This is also true for the cooperation with Dr. Reinhard Scholz who taught me to try to develop a deep understanding of the matter. Discussions with hims have always been fruitful and brought me forward.

Special thanks goes to my former as well as current colleagues from the Newdev group. To name a few: Philipp Siebeneicher, Dr. Hans Kleemann, Dr. Max. L. Tietze, Merve Anderson, Dr. Sylvia Nicht, Felix Kaschura, Dr. Changhun Yun, Robby Janneck, Kathleen Schmidt, Ji-Ling Hou, Martin Schwarze, Alrun Aline Günther, Markus Klinger, Manuel Pfalz, and Dr. Daniel Kasemann, who took over the Newdev group in the period of writing this thesis.

The results achieved would not have been on this level without the support of the administration staff: Eva Schmidt, Jutta Hunger, Johanna Katzschner, Dr. Annette Polte, Dr. Angelika Wolf, Jitka Barm, Carla Schmidt, Christian Dr. Zschalig, and Dr. Hartmut Fröb. Equally important are people who take care about the setups, technical problems, purified materials, and ensure a smooth functioning in general: Annette Petrich, Tina Träger, Sylke Furkert, Carsten Wolf, Sven Kunze, Peter Leumer, and Kai Schmidt. For this thesis, thousands of transistors and samples have been built. The large majority of them have been fabricated by the Lesker-Team: Caroline Walde, Andreas Wendel, and Tobias Günther who shall be honored here, too.

There are also several colleagues from the IAPP who supported me doing my work: Dr. Simone Hofmann, Dr. Caroline Murawski, André Döring, Dr. Torben Menke, Dr. Johannes Widmer, Dr. Matthias Schober, Florian Wölzl, Dr. Martin Hermenau, Tobias Mönch, Janine Fischer, Frederik Nehm, Dr. Tobias Schwab, Cornelius Fuchs, Markus Fröbel, Dr. Ines Moraes de Rabelo, Dr. Guohua Xie, Ralf Raupach, Matthias Böhm, Martin Wieczorek, Christoph Sachse, Dr. Donato Spoltore, Simonas Krotkus. I would like to say Thank you!

Some special thanks go to:

- Felix Kaschura for critical comments which always have been a valuable contribution
- Dr. Max L. Tietze and Martin Schwarze for performing the UPS/XPS measurements
- Dr. Sylvio Schubert who convinced me to play more football
- Dr. Matthias Schober for providing and bugfixing his program 'MOST'
- André Döring for his contribution to the calculation of capacitances from drift-diffusion simulations
- Paul Pahner for his help at the beginning of the self-heating studies

Several investigations were only possible due to cooperation with external partners. Most important for the progress achieved were my colleagues of the Weierstraß-Institut Berlin: Dr. Annegret Glitzky, Dr. Thomas Koprucki, Dr. Klaus Gärtner, Dr. Duy Hai Hoan, Dr. Jürgen Fuhrmann, and Dr. Matthias Liero. I am sure that without them "S"-shaped NDR would be still unknown for organic semiconductors. Our discussions were always fruitful and helped me to develop a critical second perspective. Further support I got shall not be forgotten:

- Dr. Thomas Gemming (IfW Dresden)
- Dr. Christoph Hossbach (IHM Dresden)
- Sebastian Eckhardt (IWS Dresden)
- Dr. Stefan Slesazeck (NaMLab gGmbH Dresden)
- Dr. Claus Luber, Dr. Jacqueline Brückner, and Dr. Michael Törker (Fraunhofer FEP/COMEDD Dresden)
- Dr. Kion Norrman (Risø DTU National Laboratory for Sustainable Energy)
- Dr. Bahman Kheradmand Boroujeni (CCN Dresden)
- Ellen Kern and Susanne Goldberg (Physikalische Chemie, TU Dresden)
- Dr. Jan Blochwitz-Nimoth (Novaled Dresden)

Finally, I would like to thank my family and my friends for their continuous support during the time I wrote my PhD thesis. Thank you so much!

ERKLÄRUNG

Diese Dissertation wurde am Institut für Angewandte Photophysik der Fakultät Mathematik und Naturwissenschaften an der Technischen Universität Dresden unter wissenschaftlicher Betreuung von Prof. Dr. Karl Leo angefertigt.

Hiermit versichere ich, dass ich die vorliegende Arbeit ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel angefertigt habe. Die aus fremden Quellen direkt oder indirekt übernommenen Gedanken sind als solche kenntlich gemacht. Die Arbeit wurde bisher weder im Inland noch im Ausland in gleicher oder ähnlicher Form einer anderen Prüfungsbehörde vorgelegt. Weiterhin versichere ich, dass keine früheren Promotionsverfahren stattgefunden haben.

Ich erkenne die Promotionsordnung der Fakultät Mathematik und Naturwissenschaften an der Technischen Universität Dresden vom 23.02.2011 an.

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Dresden, den 18.12.2014